REVISIONS			
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J.A.	5/14/85	PCN PDC-006	P1
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ICM-3216 CPU Board Specification

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1. Introduction

The ICM-3216 CPU board contains all non-memory functions for the ICM-3216 computer. The ICM-3216 is a complete computer system on two, double Eurocard size, printed circuits boards. All functions, such as CPU, memory, disk interface and I/O are contained on the ICM-3216 board set. One of these boards is the CPU module which contains the NS32016 CPU cluster, boot EPROM, four serial interfaces, address mapping logic, SCSI interface, time of day clock / calendar, real-time clock, parallel printer interface, and MiniBus interface.

The other board is a memory board designed to accept either 64K or 256K dynamic RAMs, providing 1 to 4 million bytes of memory with parity. The system design will permit a maximum of two memory boards, each having the same RAM device types, to be installed at once. This provides 2 MB maximum with 64K RAMs or 8 MB maximum with 256K RAMs. The memory board is specified in document 426010290-000.

The CPU board includes an NS32016 Central Processing Unit (CPU), NS32082 Memory Management Unit (MMU), NS32202 Interrupt Control Unit (ICU), NS32201 Timing Control Unit (TCU) and an NS32081 Floating Point Unit (FPU). The CPU cluster will operate at speeds of up to 10 megahertz and will require no WAIT states for uncontended dynamic RAM access (access to RAM on the memory board.)

Interface to hard disk, floppy disk, tape unit and other desired peripherals not specifically provided for will be via the Small Computer System Interface (SCSI). SCSI will be controlled by an I/O channel controller that supports the full (asynchronous) SCSI, including arbitration and reconnection. This interface operates only as an initiator on the SCSI bus. The peripheral(s) tied to this bus operate as targets. This interface will be implemented using an LSI SCSI device and an eight-bit microprocessor. This will provide complete control over the SCSI interface by the 32016 CPU while freeing it from controlling the many phases and details associated with management of the interface.

Data transactions between the dynamic RAM and a SCSI target will be accomplished with direct memory access of 16-bit word transfers. This should permit 1.0 megabyte per second transfers in or out of dynamic RAM yet still permit the CPU access to the dynamic RAM an average of 50 percent of the time during target transfers.

2. Features and Options

2.1. Features

The features of the ICM-3216 CPU board include:

- NS32016 Central Processing Unit, NS32082 Memory Management Unit, NS32081 Floating Point Unit, operating at 10 Megahertz with no wait states.
- Four RS-232C Ports.
- Parallel output port, supports "Centronics" interface.
- Battery operated time-of-day clock with calendar.
- MiniBus interface using MBIC.
- Full SCSI interface, asynchronous data transfers only, arbitration and reconnection for overlapped seeks and read/write operations. Eight-bit CPU for I/O channel interface control.
- 1.0 Megabyte per second SCSI (disk) transfer rate to dynamic RAM, while still permitting interleaved CPU access to dynamic RAM.
- I/O channel interface utilizes address tables for large

block transfers without main CPU (NS32016) intervention.

- Five software controllable LED indicators, each can be individually turned on or off.
- Boot EPROM sockets for 16 to 128 kilobytes (single pair of 2764, 27128, 27256 or 27512 devices.)
- NS32016 non-maskable interrupt generated by MiniBus (which includes Power Fail), memory board parity error or NS32082 MMU.
- Vectored interrupt level dedicated to each of the following (listed in descending priority):

0	Debug.
1	Software.
2	Receiver Ready, two RS-232C channels.
3	Software.
4	Receiver Ready, two RS-232C channels.
5	Software.
6	Real time clock / Test mode input.
7	Software.
8	MBIC Interrupt
9	Software.
10	Serial port interrupts, two RS-232C channels.
11	Software.
12	Serial port interrupts, two RS-232C channels.
13	I/O Channel Controller.
14	Parallel Port.
15	Software.

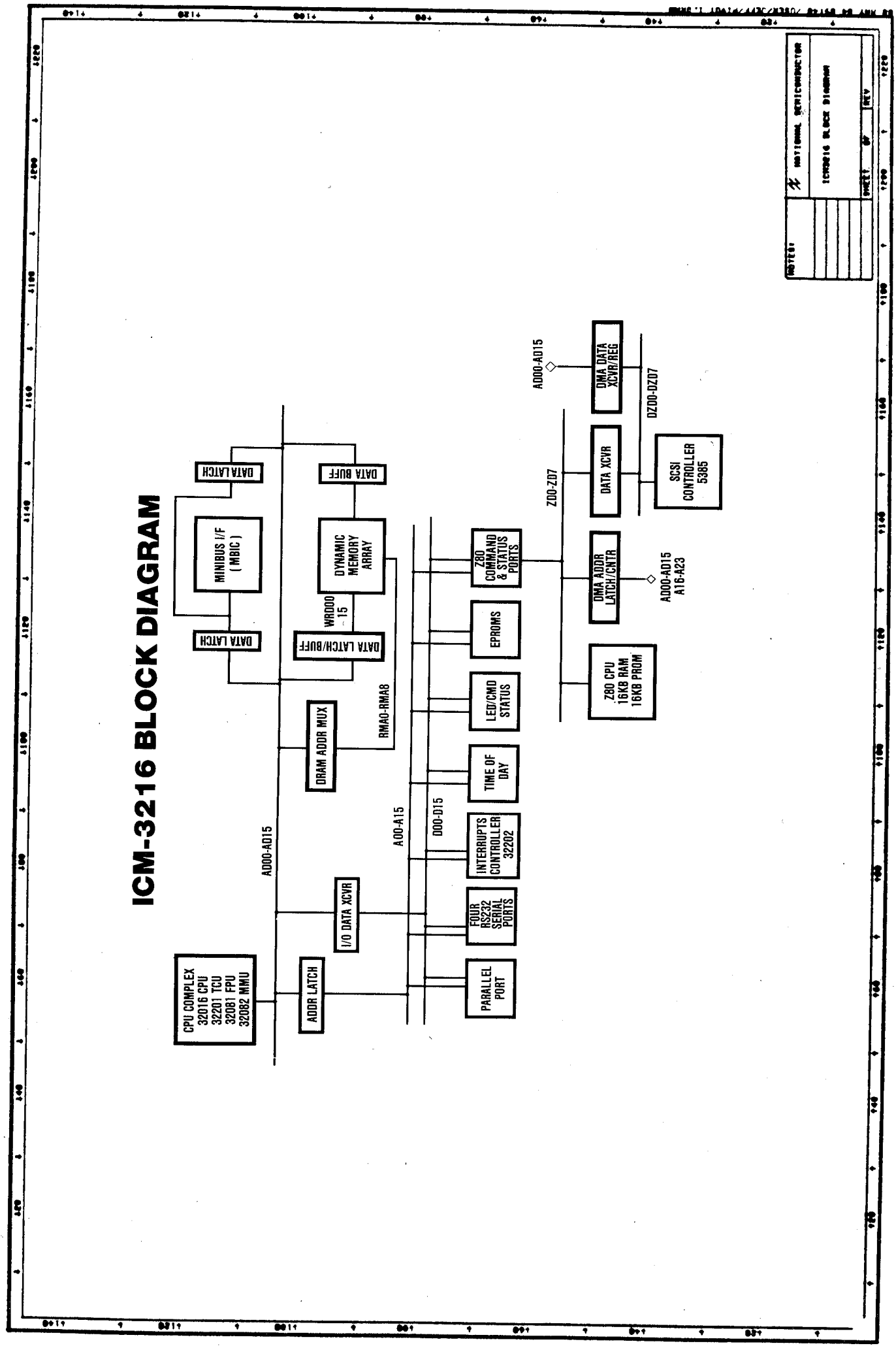
2.2. Options

The following options will be selectable:

- Each RS-232C can be configured as data terminal equipment (DTE) or data communication equipment (DCE) for direct connection to modem or terminal, respectively.
- Supports up to two memory boards (8 MB).

3. Functional Block Diagram.

Figure 3.1 shows the functional block diagram of the ICM-3216 CPU board.


ICM-3216 BLOCK DIAGRAM
CPU COMPLEX
32016 CPU
32201 TCU
32081 FPU
32082 MMU
ADDR LATCH
I/O DATA XCVR
ADD0-AD15
A00-A15
D00-D15
DRAM ADDR MUX
RMA0-RMA8
DATA LATCH
MINIBUS I/F
(MBIC)
DATA LATCH
DATA BUFF
DYNAMIC
MEMORY
ARRAY
WRD00
15
DATA LATCH/BUFF
FOUR
RS232
SERIAL
PORTS
INTERRUPTS
CONTROLLER
32202
TIME OF
DAY
LED/CMD
STATUS
EPROMS
Z80
COMMAND
& STATUS
PORTS
PARALLEL
PORT
Z00-Z07
ADD0-AD15
DMA DATA
XCVR/REG
DZD0-DZD7
DATA XCVR
SCSI
CONTROLLER
5385
DMA ADDR
LATCH/CNTR
ADD0-AD15
A16-A23
Z80 CPU
16KB RAM
16KB PROM

4. Physical Description

The ICM-3216 CPU board is fabricated on an 11.020 inch by 9.180 inch printed circuit board. Figure 7.1 illustrates an outline of the board with its dimensions and connector designations.

Physical Characteristics:

Width:	11.020 in. (28.0 cm.)
Height:	9.180 in. (23.3 cm.)
Depth:	0.625 in. (1.85 cm.)

5. Interface Pin Signal Lists and Descriptions

5.1. P1 - Parallel Printer Port

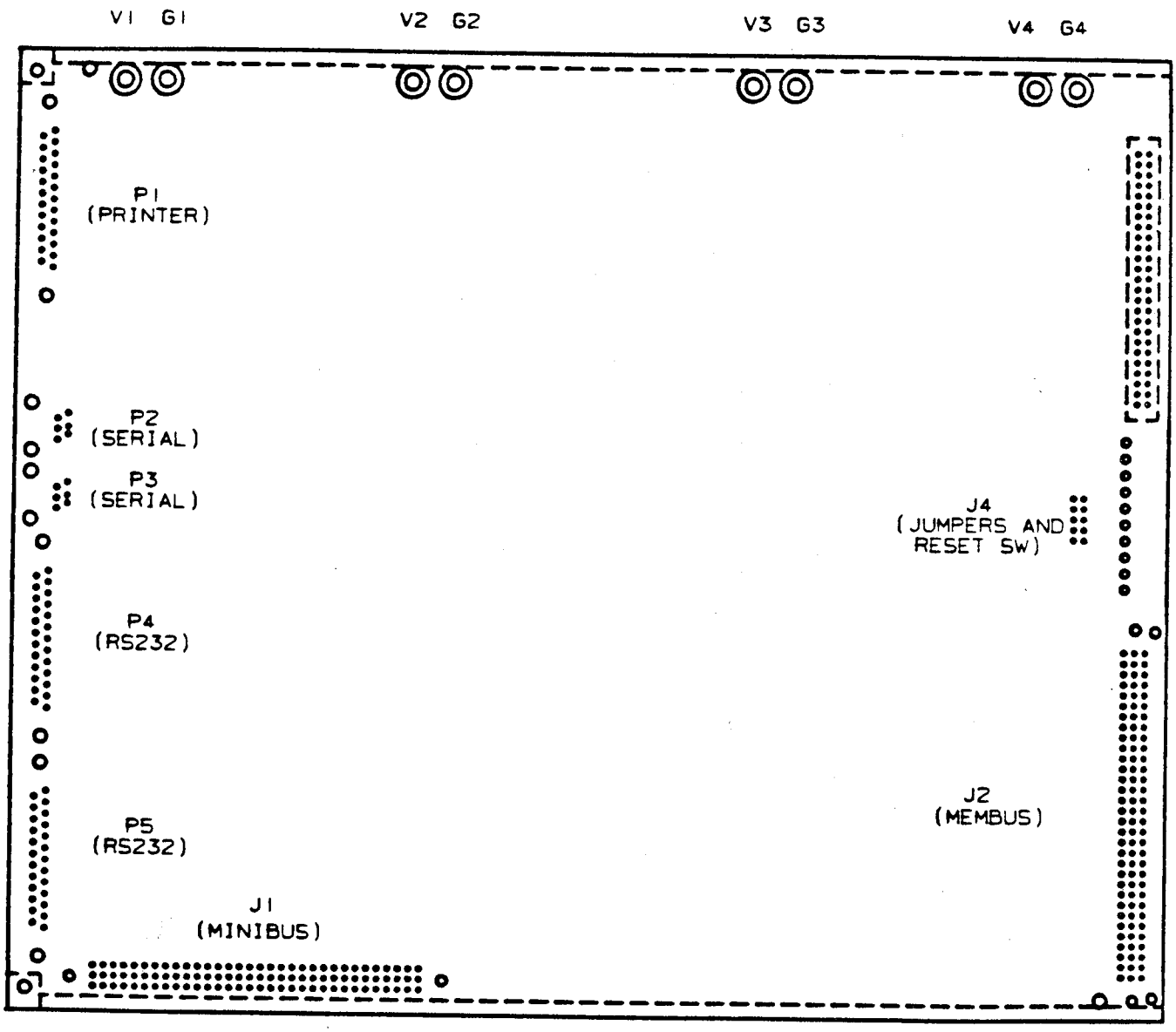
Pin assignments for the parallel printer port are defined in Table 4.1. The function of the individual signals are listed below.

PIN	MNEMONIC	PIN	MNEMONIC
1	STROBE*	14	AUTO_FD_XT*
2	DATA 1	15	ERROR*
3	DATA 2	16	INIT*
4	DATA 3	17	SELECT_IN*
5	DATA 4	18	GND
6	DATA 5	19	GND
7	DATA 6	20	GND
8	DATA 7	21	GND
9	DATA 8	22	GND
10	ACK*	23	GND
11	BUSY	24	GND
12	PE	25	GND
13	n.c.		

Table 4.1.

P1 - Parallel Printer Port Pin Assignments.

MNEMONIC	DIRECTION	SIGNAL DESCRIPTION
STROBE*	Output	Strobe pulse for data write. DATA must be valid a setup time before the negative transition of STROBE* and a hold time after the positive transition of STROBE*.
DATA1-DATA8	Output	Parallel printer data, DATA1 is the least significant bit, DATA8 is the most significant bit.
ACK*	Input	Acknowledge signal. A low pulse indicates that data has been received by the printer.
BUSY	Input	Busy signal. Set high when printer not ready



ICM-3216 CPU BOARD

		to accept another character, when printer off line or during printer error.
PE	Input	Paper End. Set high by printer to indicate paper end condition.
SELECT_IN*	Output	Select In. Must be low to select printer for operation.
INIT*	Output	Initialize. When set low, forces printer to reset to initial power-on state.
ERROR*	Input	Error. Set low by printer to indicate error condition, including: 1. Paper End. 2. Off line. 3. Error state.
AUTO_FD_XT*	Output	Auto feed. When set low, an automatic line feed is performed each time a carriage return is received by the printer.

5.2. RS-232C Ports - P2 & P3

Table 4.3 shows the connector P2 & P3 pin assignments and descriptions of the interface signals.

PIN	MNEMONIC	SIGNAL DESCRIPTION
A	U_MAY_SEND	Output handshake to enable input data transmission.
1	GND	Ground.
2	U_SEND_DATA	Input serial data.
3	I_SEND_DATA	Output serial data.
4	GND	Ground.
B	I_MAY_SEND	Input handshake to enable output data transmission.

Table 4.3.

Connectors P2 & P3 - RS-232C Interface Pin Signal List.

5.3. RS-232C Ports - P4 & P5

Table 4.4 shows the connector P4 & P5 pin assignments and descriptions of the interface signals.

PIN	MNEMONIC	DTE	DCE	SIGNAL DESCRIPTION
1	GND			Protective Ground
2	TXD	O	I	Transmitted Data
3	RXD	I	O	Received Data
4	RTS	O	I	Request to Send
5	CTS	I	O	Clear to Send
6	DSR	I	O	Data Set Ready
7	SGND			Signal Ground
8	RLSD	I	O	Receive Line Signal Detect
9	n.c.			
10	n.c.			
11	n.c.			
12	n.c.			
13	n.c.			
14	n.c.			
15	n.c.			
16	n.c.			
17	n.c.			
18	n.c.			
19	n.c.			
20	DTR	O	I	Data Terminal Ready
21	n.c.			
22	n.c.			
23	n.c.			
24	n.c.			
25	n.c.			

where: I = Input, O = Output

Table 4.4.

Connectors P4 & P5 - RS-232C Interface Pin Signal List.

5.4. MiniBus Interface - J1

The MiniBus interface is provided thru the MiniBus Interface chip (MBIC). This single CMOS LSI component attaches directly to the 32016 bus and provides a complete interface to a sophisticated 16-bit bus.

MiniBus is a 16-bit bus with full support for multiple processors complete with parity on address/data lines and physical addressing of all MiniBus masters (8 maximum). The MBIC provides a path for the IOC's on the MiniBus to directly access the IOP's memory as required for the individual functionalities, as well as the ability to exchange interrupts between any pair of masters to co-ordinate the activities.

Interlocked operations are supported on the MiniBus to allow management of queues by independent processing units.

Refer to the MiniBus Specification (426600019-000) and the MBIC Specification (426600020-000) for complete information on the bus discipline and the component.

MiniBus Connector Pinout (J1)

c01 - gnd	b01 - +12V	a01 - gnd
c02 - BUSPAR	b02 - +12V	a02 - BUSERR*
c03 - BA20	b03 - +12V	a03 - IO*
c04 - BA19	b04 - +15V	a04 - BA21
c05 - BCOD0*	b05 - gnd	a05 - BCOD1*
c06 - gnd	b06 - gnd	a06 - gnd
c07 - BA16	b07 - +5V	a07 - BA18
c08 - BA17	b08 - +5V	a08 - BA02
c09 - BA03	b09 - +5V	a09 - BA00
c10 - BA01	b10 - gnd	a10 - BA04
c11 - gnd	b11 - gnd	a11 - gnd
c12 - BA05	b12 - +5V	a12 - BA06
c13 - BA07	b13 - +5V	a13 - RESET*
c14 - BREQ0*	b14 - +5V	a14 - BREQ1*
c15 - BREQ2*	b15 - HOLD*	a15 - BREQ3*
c16 - BREQ4*	b16 -	a16 - BREQ5*
c17 - gnd	b17 -	a17 - BREQ7*
c18 - BCLK	b18 - gnd	a18 - gnd
c19 - gnd	b19 - gnd	a19 - gnd
c20 - GABCLK	b20 - gnd	a20 - gnd
c21 - gnd	b21 - gnd	a21 - gnd
c22 - BCLK/2	b22 - INT07	a22 - gnd
c23 - BREQ6*	b23 - INT06	a23 - PFAIL*
c24 - RFRTIM	b24 - INT05	a24 - PWAIT*
c25 - INT03	b25 - INT04	a25 - INT02
c26 - INT01	b26 - +5V	a26 - INT00
c27 - gnd	b27 - +5V	a27 - gnd
c28 - BA12	b28 - gnd	a28 - BA14
c29 - BA09	b29 - -15V	a29 - BA15
c30 - BA11	b30 - -12V	a30 - BA08
c31 - BA13	b31 - -12V	a31 - BA10
c32 - gnd	b32 - -12V	a32 - gnd

Table 4.5.

J1 - MiniBus Pin assignments

5.5. MemBus - J2

Connector J2 connects the CPU board to the Memory board or boards. Pin assignments for this connector are summarized in Table 4.6.

MemBus Connector Pinout (J2)		
c01 - gnd	b01 - RAST	a01 - gnd
c02 - gnd	b02 - gnd	a02 - gnd
c03 - MSHADOW	b03 - RD*	a03 - HLDD-RD
c04 - HA2*	b04 - HA3*	a04 - A23
c05 - HA0*	b05 - +5V	a05 - HA1*
c06 - gnd	b06 - +5V	a06 - gnd
c07 - WRMEML	b07 - gnd	a07 - WRMEMH
c08 - gnd	b08 - gnd	a08 - gnd
c09 - gnd	b09 - CAST	a09 - gnd
c10 - gnd	b10 - +5V	a10 - gnd
c11 - REFRESH*	b11 - gnd	a11 - gnd
c12 - 64K*	b12 - RMA0	a12 - gnd
c13 - RMA1	b13 - RMA2	a13 - RMA3
c14 - gnd	b14 - +5V	a14 - gnd
c15 - RMA4	b15 - RMA5	a15 - RMA6
c16 - RMA7	b16 - gnd	a16 - RMA8
c17 - gnd	b17 - AD00	a17 - gnd
c18 - AD01	b18 - AD02	a18 - AD03
c19 - AD04	b19 - gnd	a19 - AD05
c20 - AD06	b20 - AD07	a20 - AD08
c21 - gnd	b21 - AD09	a21 - gnd
c22 - AD10	b22 - AD11	a22 - AD12
c23 - AD13	b23 - gnd	a23 - AD14
c24 - AD15	b24 - RDDP1	a24 - RDDP0
c25 - gnd	b25 - WRDP1	a25 - gnd
c26 - WRDP0	b26 - WRD00	a26 - WRD01
c27 - WRD02	b27 - gnd	a27 - WRD03
c28 - WRD04	b28 - WRD05	a28 - WRD06
c29 - gnd	b29 - WRD07	a29 - gnd
c30 - WRD08	b30 - WRD09	a30 - WRD10
c31 - WRD11	b31 - gnd	a31 - WRD12
c32 - WRD13	b32 - WRD14	a32 - WRD15

Table 4.6.

J2 - MemBus pin assignments

MNEMONIC	SIGNAL DESCRIPTION
AD15 - AD00	Read Data, bits 15 through 00. Data word read from RAM.
WRD15 - WRD00	Write Data, bits 15 through 00. Data word written to RAM.
RMA8 - RMA0	RAM Address, bits 8 through 0. Represents RAM row address or column address. RMA8 is used only with 256K RAMs.
RAST	Row Address Strobe. Indicates RMA8 - RMA0 is row address.
CAST	Column Address Strobe. Indicates RMA8 - RMA0 is column address.
WRMEMH	Write Memory High. Asserted when writing the

high-order data byte to memory.

WRMEML	Write Memory Low. Asserted when writing the low-order data byte to memory.
REFRESH~	Refresh, active-low signal. Asserted during a refresh cycle.
MSHADOW	Memory Shadow. Generated by CPU board; set upon power-up, cleared upon memory access with A23 = 1. When set, prevents RAM access, allowing CPU board EPROM to occupy low address space.
HA0~ - HA3~	High-Order Address. Represents CPU address bits 17 through 20 when using 64K RAMs; bits 19 through 22 when using 128K RAMs.
A23	CPU Address 23. Must be low for RAM access.
64K~	64K RAM. A jumper-set low level indicates that the memory board uses 64K RAMs; a high level indicates 128K RAMs.
RD~	Read. Asserted when reading data from memory.
HLDD_RD~	Hold Data Read. Extends read data valid beyond RD~.
RDDP0, RDDP1	Read Parity. Low-order byte and high-order byte parity bits read from memory.
WRDP0, WRDP1	Write Parity. Low-order byte and high-order byte parity bits written to memory.

5.6. Power Connector - J3

Connector J3 contains Power Interface signals and voltages in addition to those provided over the V1-4 and G1-4 connectors. Table 4.7 lists these signals and their pin assignments.

PIN	MNEMONIC	SIGNAL DESCRIPTION
1	GND	Ground
2	+5V	+5 Volt Power
3	RESET*	System Reset (optional)
4	POWER_FAIL*	Power Fail Interrupt (optional)
5	GND	Ground
6	-12V	-12 Volt Power
7	+12V	+12 Volt Power
8	GND	Ground
9	+5V	+5 Volt for Power Switch LED
10	REMOTE_OFF*	Remote_off* signal from power switch

Table 4.7.

J3 - Power Interface Connector.

Note: In order to guarantee the integrity of data in the Time of Day Chip, the POWER-FAIL* signal must be true (low) for at least 100 microseconds after +5VDC is stable on power-up, and must be true at least 100 microseconds prior to +5VDC beginning to drop in power-down or during a power failure.

5.7. J4 - Reset & Indicator Interface.

J4 provides an interface to an externally mounted SPDT reset switch and LED indicators. These five indicators will operate in parallel with the five LED indicators on the board. Pin definitions and signal descriptions are shown in Table 4.8.

PIN	MNEMONIC	SIGNAL DESCRIPTION
1	SWNO	Reset switch normally open contact
2	SWCOM	Reset switch common contact
3	SWNC	Reset switch normally closed contact
4	LEDPWR	+5 volt power for LED indicators
5	LED1	LED 1 Cathode connection
6	LED2	LED 2 Cathode connection
7	LED3	LED 3 Cathode connection
8	LED4	LED 4 Cathode connection
9	LED5	LED 5 Cathode connection, MiniBus Reset* indicator
10	n.c.	No connection

Table 4.8.

J4 - Reset & Indicator Interface.

5.8. J5 - Small Computer System Interface.

Pin assignments for the Small Computer System Interface (SCSI) are described in Table 4.9. A description of the functions of the individual functions is given below.

PIN	MNEMONIC	PIN	MNEMONIC
1	gnd	2	DB(0)*
3	gnd	4	DB(1)*
5	gnd	6	DB(2)*
7	gnd	8	DB(3)*
9	gnd	10	DB(4)*
11	gnd	12	DB(5)*
13	gnd	14	DB(6)*
15	gnd	16	DB(7)*
17	gnd	18	DB(P)*
19	gnd	20	gnd
21	gnd	22	gnd
23	gnd	24	gnd
25	gnd	26	TERMPWR
27	gnd	28	gnd
29	gnd	30	gnd
31	gnd	32	ATN*
33	gnd	34	gnd
35	gnd	36	BSY*
37	gnd	38	ACK*
39	gnd	40	RST*
41	gnd	42	MSG*
43	gnd	44	SEL*
45	gnd	46	C/D*
47	gnd	48	REQ*
49	gnd	50	I/O*

Table 4.9.

J5 - SCSI Pin Assignments.

MNEMONIC	DIRECTION	SIGNAL DESCRIPTION
DB(0)* to DB(7)*	I/O	Data bus. Negative true data bus, DB(0)* is the least significant bit, DB(7)* is the most significant bit.
DB(P)*		Data bus odd parity bit.
BSY*	I/O	Busy. An "or-tied" signal which indicates that the bus is being used.
SEL*	I/O	Select. A signal used by an Initiator to select a Target or by a Target to reselect an initiator.
C/D*	Input	Command / data. A signal driven by a Target which controls the direction of data movement on the data bus with respect to an Initiator.
MSG*	Input	Message. A signal driven by a Target during the MESSAGE phase.

REQ*	Input	Request. A signal driven by a Target to indicate a request for a REQ/ACK data transfer handshake.
ACK*	Output	Acknowledge. A signal drive by an Initiator to indicate an acknowledgement for a REQ/ACK data transfer handshake.
ATN*	Output	Attention. A signal driven by an Initiator to indicate the ATTENTION condition.
RST*	I/O	Reset. An "or-tied" signal which indicates the RESET condition.
TERMPWR	Output	Terminator Power. +5V that can be used for terminators or testing.

6. Interface Timing Specifications

Table 5.1 lists the timing specifications for the serial RS-232C interface connectors P2 through P5 and the parallel printer port, P1. The timing diagram for P2 through P5 is shown in Figure 5.1 while the timing diagram for P1 is shown in Figure 5.2.

Table 5.2 lists the timing specifications for the J5 SCSI port. Figure 5.3 shows the timing diagram for SCSI

Parameter	Min. (us)	Max. (us)	Description	Remarks
tBIT	26	14 msec.	Bit time	RS-232C Serial Port
tPAW	5		ACK* strobe width	Parallel Printer Port
tPDS	1		Data setup time	"
tPDH	1		Data hold time	"
tPSW	1		STROBE* width	"

Table 5.1.

J1-J4 & J6 Timing Specifications.

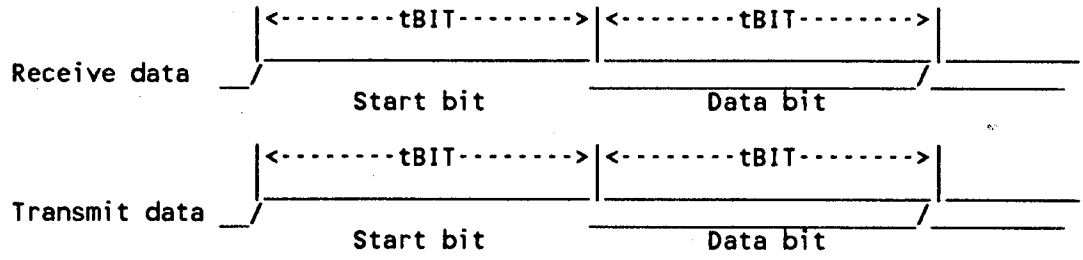


Figure 5.1.

ICM-3216 CPU board Serial I/O Timing.

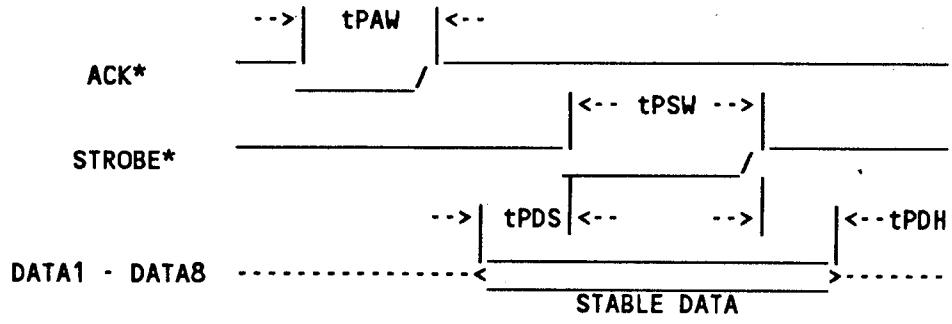


Figure 5.2.

Parallel Port J6 Timing Diagram

Parameter	Min. (ns)	Max. (ns)	Description
tSBD	800	1800	Bus free / bus set delay
tSAD	2200		Arbitration delay
tSCD	800		Bus clear delay
tSRP	25000		Reset pulse width

Table 5.2.

J7 - SCSI Timing Specifications.

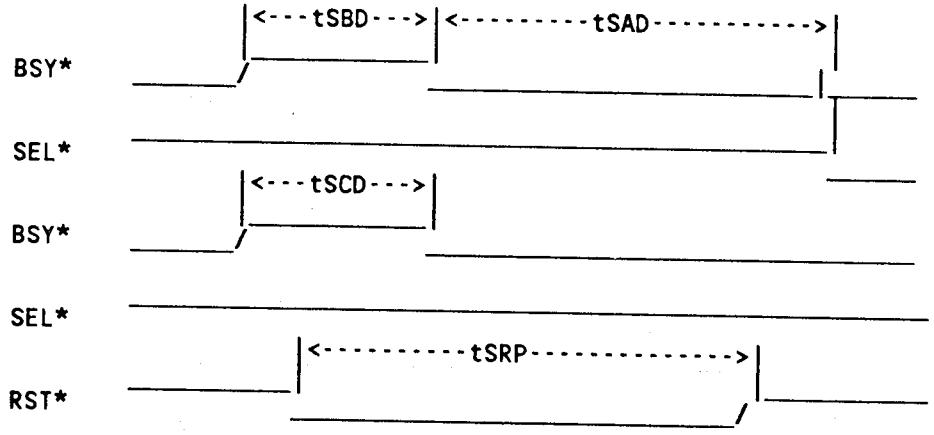


Figure 5.3.

J7 - SCSI Timing Diagrams.

7. Software Interface Definition

7.1. Address Map

7.1.1. RAM Addressing

The RAM always begins at address 000000 (hex) and is contiguous up to the ending address. The ending address is dependent upon the amount of RAM installed according to the following table:

Configuration	RAM size	RAM address space
1 Memory bd., 64K devices	1 MB	0 to 0fffff
1 Memory bd., 256K devices	1 MB	0 to 0fffff
2 Memory bds., 64K devices	2 MB	0 to 1fffff
1 Memory bd., 256K devices	2 MB	0 to 1fffff
1 Memory bd., 256K devices	4 MB	0 to 3fffff
2 Memory bds., 256K devices	8 MB	0 to 7fffff

Note that while the MSHADOW flip-flop is asserted, RAM cannot be read, only written (See ROM addressing, Sec. 6.1.2).

7.1.2. ROM Addressing

At power-up or after assertion of RESET*, a flip-flop with the signal name MSHADOW is asserted. When MSHADOW is asserted, the PROM can be read from a starting address of 0 (hex) (which "shadows" the RAM) or 800000. When MSHADOW is cleared, the PROM can no longer be read from starting address 0 and is only readable starting at 800000. MSHADOW is cleared by the first CPU access with the most significant address bit (A23) set to a one. Note that when MSHADOW is cleared, the PROM starting at address 0 "disappears" and caution must therefore be exercised to be sure the CPU program counter is pointing to the desired program before clearing MSHADOW.

(NOTE: A20 is a don't care in the PROM address decode logic, thus a starting adddress of 900000 could be substituted for 800000 in the above description.)

7.1.3. I/O Addressing

The following table defines the base address for all I/O devices. The eight-bit ports use only even addresses so multiple registers for a single device are offset from the base address in increments of two.

I/O ADDRESS	READ	WRITE
A00000	Real Time Clock	Real Time Clock
A00020	DUART #1 (P4 & P5)	DUART #1 (P4 & P5)
A00040	DUART #2 (P2 & P3)	DUART #2 (P2 & P3)
A00080	Printer Status	Printer Output Data
A00082		Printer Command
A000A0	I/O Channel Status	I/O Channel Command
A000C0	NM Interrupt Status	LED / Control Reg.
A000E0	Enable NMI	MBIC Map Address
C00000 to FFC000	MBIC	MBIC
FFFE00	Interrupt Controller	Interrupt Controller

7.2. I/O Channel Controller

7.2.1. Introduction

An I/O channel controller handles the physical path management between the main CPU (host) and target disk or tape device. This channel controller handles the details of SCSI including arbitration, selection, disconnection and reconnection. The host CPU is in complete control of the device at the other end of the SCSI bus. The host will place a command descriptor block (as defined by SCSI) in memory. The I/O channel controller will acquire the SCSI bus (arbitration and selection phases), copy the command to the target, manage the transfer, and then interrupt the host CPU when the target sends the command complete message. The I/O channel controller does no interpretation of the commands or data transmitted between the host and the target, it only manages the transfer. This results in the full power of the SCSI command structure available to the host without the overhead of the SCSI physical path management.

The SCSI bus can be connected to one of seven target controllers. Each target controller can control up to eight logical devices. The I/O channel controller supports several subchannels operating concurrently. Each subchannel can control a separate logical device on the SCSI bus. This will permit overlapped disk operations for read, write, seek etc. The number of subchannels supported will be eight.

The I/O channel controller is initialized by I/O commands but actual subchannel target commands are controlled by an IOCB (I/O control block) in main memory. Once the host sets up the command in memory, the I/O channel will complete the command and then interrupt the host upon completion. The host can then examine the IOCB(s) to check for errors or proper completion.

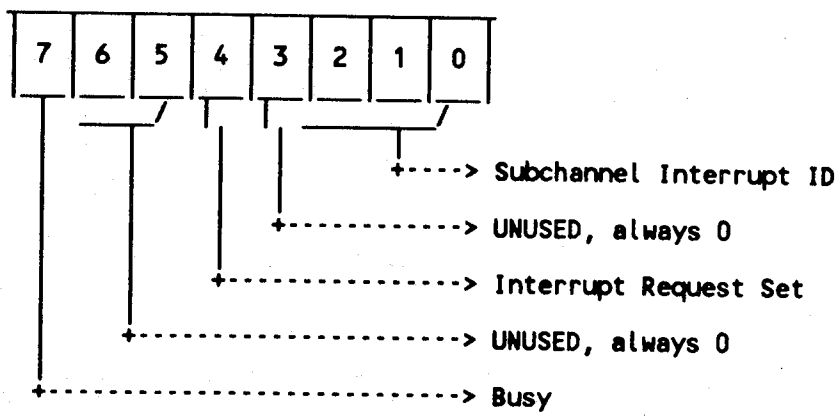
If the target controller supports linked command complete with flags, then the I/O channel controller will only interrupt the host upon receiving a linked command complete with flag or a command complete message.

7.2.2. I/O Interface

I/O-mapped command and status registers provide communication between the host CPU and channel controller. The commands are:

Command #	I/O Command Description
00	Write Command Pointer Table physical address (three byte address follows to command register, LSB first)
01	Interrupt acknowledge. Clear interrupt request. Must be issued after reading status register to determine source of interrupt.
02	Reset I/O channel controller.
03	Reset SCSI
04	Execute diagnostic firmware.
1n	Start I/O, subchannel n. Begin I/O operations on subchannel n, using IOCB pointed to by appropriate Command Pointer Table Entry.
2N	Abort I/O, subchannel n. Abort I/O operations on subchannel n. If subchannel n is not active or the I/O has completed, this command is ignored, otherwise, I/O is aborted and the abort I/O channel error status code is returned.

The I/O status byte is defined as:



The busy bit is used to synchronize the multi-byte command (command 0) and indicate status byte not yet updated. It is set (by hardware) by a command write and cleared by the I/O controller.

7.2.3. Command Pointer Table

The Command Pointer Table (CPT) is a table resident in main memory that is set up by the host to communicate to the I/O channel controller the address of an IOCB for target command execution or a channel command for specific I/O channel controller commands. There is one entry in the CPT for each subchannel. Each entry is as follows:

BYTE	DESCRIPTION
0..2	Physical address of an IOCB or Channel Command
3	Unused by I/O channel controller.

Note: The address of the IOCB in the CPT is not updated by the I/O channel controller during command or linked command execution. Therefore, during execution of a series of linked commands by the I/O channel controller, the CPT entry will always point to the first command in the link, not the currently executing command.

7.2.4. I/O Control Block (IOCB)

The IOCB defines SCSI commands to be executed by the target device. Byte 0 having a value of zero defines this as an IOCB. The format of the IOCB is as follows:

BYTE(S)	DESCRIPTION
0	Byte 0 must always contain the value 0
1	bit 7 = 0 bit 6..4 = Target Device I.D. bit 3 = 0 bit 2..0 = Logical Unit Number
2..13	Command Descriptor Block (CDB as defined by SCSI)
14	Status byte returned from SCSI target device (Only assured to be valid when I/O channel controller error status code is 0.)
15	I/O channel controller error status code.
16..19	Data pointer. Pointer to data to be transferred. The low order 9 bits (bits 0..8) point to the byte within the page of the next word to be transferred. Bits 9..23 are an index into the transfer pointer table for the physical page address. Normally, a transfer would begin with bits 9..23 all zero so that the first transfer pointer table entry is used for the first data transfer of a block. If the final byte written is even (i.e. the pointer is odd upon completion), the contents of the odd byte beyond the pointer will be altered.
20..23	Transfer pointer table address. Physical address of table of physical addresses for data transfer. Each entry points to the base of a 512-byte page, thus the low order nine bits (0..8) of entries in this table are ignored by the I/O controller. The high order eight bits (24..32) of entries in this table are also ignored, so MMU Page tables could be used. If the transfer pointer value is zero (all 32 bits), then the data pointer is a physical address and no table is used.
24..27	Transfer limit. Limit on number of bytes to transfer. Value of zero sets the limit to 1 Megabyte. It is highly recommended that a non-zero value always be entered for translated transfers as the transfer limit value determines how many entries in the translation table must be copied to I/O controller memory. For reads from SCSI, this transfer limit will control how much host memory will be written. For writes, a disk can be written beyond the transfer

limit.

28..31 Link pointer (physical address). Pointer to linked command (only used if I/O controller receives Linked command complete message from target.)

NOTE: The IOCB, Command Descriptor Block, and transfer pointer table must begin on an even byte address (i.e. be word aligned). The number of bytes to transfer (Residual count and transfer limit) must be even.

7.2.5. Channel Commands

When the first byte of the command pointed to by the CPT is nonzero, the command is not an IOCB but a channel command. No channel commands are presently defined.

NOTE: Channel command must begin at an even byte address (word aligned).

7.3. I/O Channel Error Status Codes

The I/O Channel Error Status Codes returned in the IOCB are as follows:

VALUE	DESCRIPTION
0	No error occurred
1	Command aborted (via Abort I/O command).
2	Selection Timeout
3	Attempt to transfer more that transfer limit bytes
4	Invalid Channel Command.
5	Insufficient buffer space for translation table required by requested transfer.
6	Unexpected disconnection by target device during command execution.

Additional error codes will be added as need arises.

7.4. MiniBus RAM Address Mapping

Access to dynamic RAM from the MiniBus is mapped from a 64K window to any 64K segment of the RAM. A map table will reside in main RAM and will contain 256 two-byte entries. The location of the table will be any 512 byte page (beginning on a page boundary.) A fifteen bit I/O mapped latch that is settable by software will define the page within memory where this table resides.

The format of the data in the table will be:

Bit 15 - Bit 9 = Page address bits 15 - 9

Bit 8 - Bit 1 = Page address bits 23 - 16
Bit 0 = Don't care

7.5. NMI Status Register

Reading from address A000C0 (hex) will return the current NMI status. This will clear any outstanding parity interrupts. The meaning of the data read is:

Bit 8 = 1 parity error (indicates bits 0..5 are valid).

Bit 7 = 1 MBIC Interrupt

Bit 6 = 1 MMU interrupt

Bit 5 = 1 parity error on odd byte.

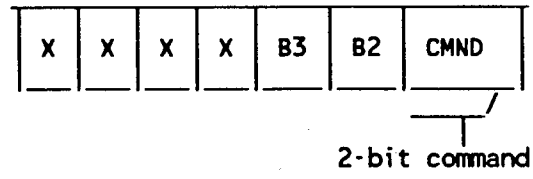
Bit 4 = 1 parity error on even byte.

Bits 3..0 = encoded to indicate which chips had parity error.

NMI must be re-enabled by a read of A000E0.

7.6. Printer Port

Three addresses are associated with the printer port. They are printer write data, printer status and printer command. The printer command is defined as follows:



COMMAND	Action
00	Set Output Mode (printer mode) INIT(Prime) = B2 SELECT_IN = B3 (Note: A "1" in control signal bit position sets interface signal low.)
01	Clear Busy (Input Mode Only) (B2,B3 = don't care)
10	Set Input Mode

The printer status register is defined as follows:

Bit 0 = AUTO_FD_XT*

Bit 1 = STROBE*

Bit 2 = INIT*

Bit 3 = SELECT_IN*

Bit 4 = ERROR*

Bit 5 = PE

Bit 6 = BUSY

Bit 7 = PRINTER_READY (Indicates hardware ready for another character or character available if in input mode.

Characters are sent to the printer by reading the status register checking for PRINTER_READY in the status register and outputing to the printer data output

port. Strobing and handshake with the printer are accomplished by the hardware.

8. Environmental Requirements

Operating temperature: 0C to +55C

Relative Humidity: to 90%, noncondensing

9. Power Requirements

Power requirements for the ICM-3216 CPU board are as follows:

Voltage	Tolerance	Maximum Current (amp.)	
+ 5 V DC	+/- 5%	6.2	
+/- 12 V DC	+/- 5%	.069	
+/- 15 V DC	+/- 5%	0	(used only by MiniBus)

10. Reliability

A comprehensive three-phase testing program has been designed to ensure that all products that are shipped will perform completely to this specification through the lifetime of this product.

The first phase is an impedance test performed on the PCB after it is assembled. The components on the board are examined through a set of tests designed to uncover any manufacturning induced malfunctions.

The second phase is functional testing. The PCB is put in an environmental chamber, and exercised with a full set of diagnostic programs. This phase is designed to weed out infant mortality, and to ensure board functionality over environmental, as well as operation extremes.

The third phase is a system configuration test. The PCB is connected to a standard system, with system level software. This phase is designed to ensure the board's functionality in a system level environment.