National Semiconductor

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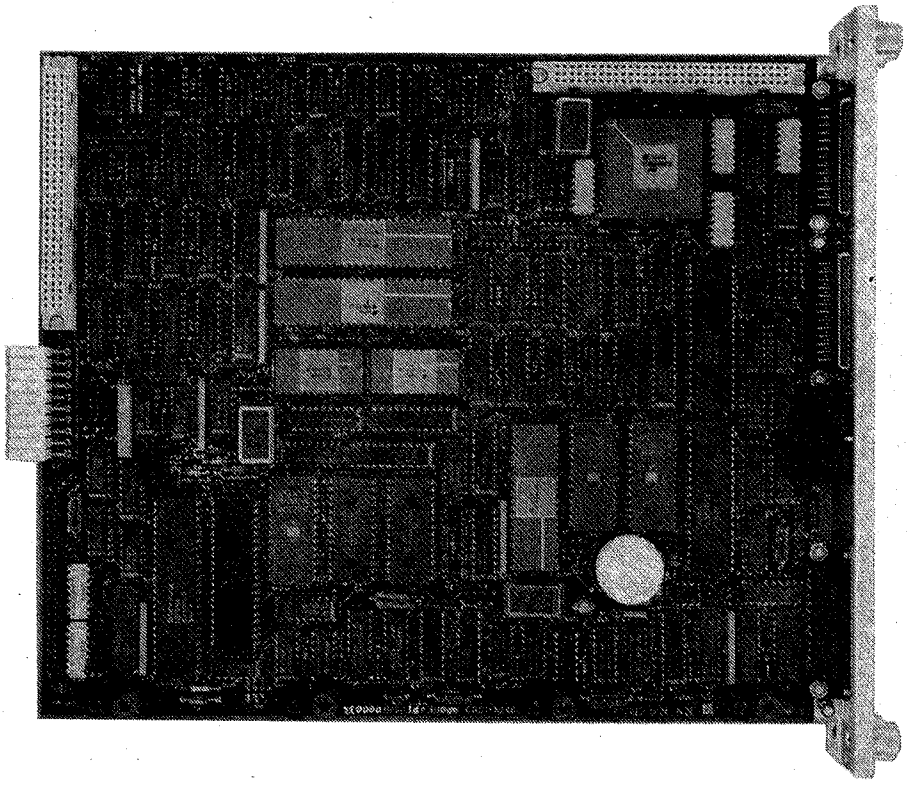
ICM-3216
Integrated Computer Module



- **Series 32000® Chip Set**
  - **— NS32016 32/16-bit Central Processing Unit**
  - **— NS32201 Timing Control Unit**
  - **— NS32082 Memory Management Unit**
  - **— NS32081 Floating Point Unit**
  - **— NS32202 Interrupt Control Unit**
- **Four asynchronous RS232C compatible serial ports**
- **Centronics compatible printer port**
- **Full SCSI Interface**
- **MiniBus I/O Interface**
- **Time of day clock/calendar with battery backup**
- **1–8 Mbytes of Random Access Memory**
- **EPROM sockets for 16k to 128k bytes of EPROM**
- **System V/Series 32000 available as an option**

Overview

Integrated Computer Modules are designed to provide "supermicrocomputer" solutions to the OEM for applications in the office automation, workstation, graphics and process control areas. These Series 32000 based modules are not designed around any industry standard bus but are, rather, designed as single board computers which access memory across a very fast private bus designed to enhance the Series 32000 operation. The modular concept employs a generic base board used by all the units along with a personality board to provide the required functionality. This improves price/performance: Price decreases because there is no need for a backplane; Performance increases because there are no wait states caused by the bus. The backplane-like quality of having configuration options is, however, maintained.

Series 32000® is a registered trademark of National Semiconductor Corporation.
UNIX™ is a trademark of AT&T Bell Laboratories.
Z80B® is a registered trademark of Zilog Corp.

DS6786S-10M16 Printed in W.Germany

Overview (Continued)

The ICM-3216 is a complete computer system contained on two 11.02 in. (280 mm) x 9.18 in. (233 mm) printed circuit boards. This Integrated Computer Module adds the power of the Series 32000 processor chip set to National Semiconductor's line of board level microcomputer products. The CPU cluster (CPU, TCU, MMU, FPU, and ICU), PROM sockets, serial interfaces, address mapping logic, SCSI interface, parallel port, memory interface and MiniBus interface reside on the CPU unit.

Up to two memory boards can be configured with the CPU unit to provide between one and eight million bytes of memory. The memory board(s) interface to the CPU unit via a "Direct Connect" local memory bus. The system operates at 10 MHz with no wait states for normal memory access.

The Integrated Computer Module is designed to operate as a single board computer and communicates with memory via a high speed local bus which circumvents the arbitration and speed problems associated with the various industry standard buses. A Small Computer Systems Interface (SCSI) provides the interface to hard disk and tape units. SCSI is implemented by using an LSI SCSI device and a Z80B® microprocessor. This provides complete control of the interface by the NS32016 CPU while freeing it from controlling the associated details of the transfer. Data transfer between the dynamic RAM and mass storage is accomplished with direct memory access of 16-bit words.

Functional Description

CPU Cluster

The Series 32000 is a complete family of 32-bit CPUs, slave processors and peripherals. All processors, Memory Management Unit and Floating Point Unit are designed with 32-bit internal buses and registers to provide a true, two address architecture. The instruction set supports fast, highly compact, compiler code making the Series 32000 ideal for use with high level languages. The Memory Management Unit offers Demand-Paged Virtual Memory and fast on-chip address translation. This makes the Series 32000 an excellent engine for the UNIX™ operating system. The Floating Point Unit provides a hardware math unit which operates up to 100 times faster than software emulation. Since all CPUs in the series 32000 line have a 32-bit internal architecture, the same software can be incorporated into all the systems within the family.

Space saving compiler code, hardware floating point support, demand-paged virtual memory and total software compatibility assure the speed, flexibility and cost effective operation needed in a system.

NS32016 CPU (Central Processing Unit)

The ICM-3216 utilizes the NS32016 as the Central Processing Unit. This CPU has a uniform linear 16 Mbyte addressing range and a full 32-bit internal architecture and implementation. Internal working registers, data paths and ALU are all 32 bits. This provides simpler handling of 32-bit data types and provides total compatibility with the next generation of 32-bit microprocessors.

The instruction set is fashioned after high level language instructions. Displacements can be 32 bits, ensuring that the instruction set will remain upward/downward compatible across the spectrum of Series 32000 CPU devices. With the Series 32000 CPU it is possible to add, subtract, multiply, divide or do any other operation with both operands in memory. This is a speed benefit for assembly code and is particularly needed in a high level language environment, since high level languages nearly always do memory-to-memory operations.

Restrictions frequently encountered, where only certain data types can be used with certain instructions, with particular addressing modes, with restricted sources and destinations, do not exist on Series 32000. ANY data type can be used with ANY instruction with ANY addressing mode with ANY source or destination. This makes the assembly programmer's task easier because there are no restrictions to track. With high level languages, the improvement becomes even more pronounced. Compilers produce very fast and efficient code when operating with a symmetrical machine.

NS32201 TCU (Timing Control Unit)

The NS32201 Timing Control Unit provides the two phase clock system, system control logic (read, write and data buffer enable) and cycle extension Logic for the Series 32000 family.

Clocks provided are a two phase, non-overlapping 10 MHz clock, and 10 and 20 MHz TTL compatible clocks.

When operating with slow peripherals, Cycle Extension is required. TCU Cycle Extension features include programmable wait state inputs, a "slow" cycle to accommodate slower peripherals and a cycle hold to allow additional time for arbitration before generating control signals.

NS32082 MMU (Memory Management Unit)

The increased requirement for development and execution of very large programs on cost effective systems has caused the development of virtual memory machines where programs larger than the physical memory space are routinely executed on the system. This is accomplished by maintaining the currently necessary portions of the program in the physical memory space and storing the remainder in mass storage. Portions of the program are switched in or out of physical memory as necessary. Since this switching operation is controlled by the operating system and is transpar-

Functional Description (Continued)

ent to the user, it appears that greater memory is available than is actually the case. Thus, "virtual" memory.

The Series 32000 uses demand-paged virtual memory, with each page containing 512 bytes. Since the physical memory is a collection of these 512 byte pages, moving from physical memory to disk or from disk to physical memory becomes relatively simple.

The NS32082 Memory Management Unit provides hardware support for demand-paged virtual memory management. Its specific capabilities include fast dynamic address translation, protection on individual 512 byte pages and detailed status to assist an operating system in efficiently managing up to 16 Mbytes of physical memory.

For the purpose of address translation, memory is divided into 512 byte pages. A virtual address for the MMU is composed of two fields: a virtual page frame number and a nine bit offset. The offset is unchanged by the translation algorithm. The MMU translates the virtual page number to a physical page number according to page tables stored in memory.

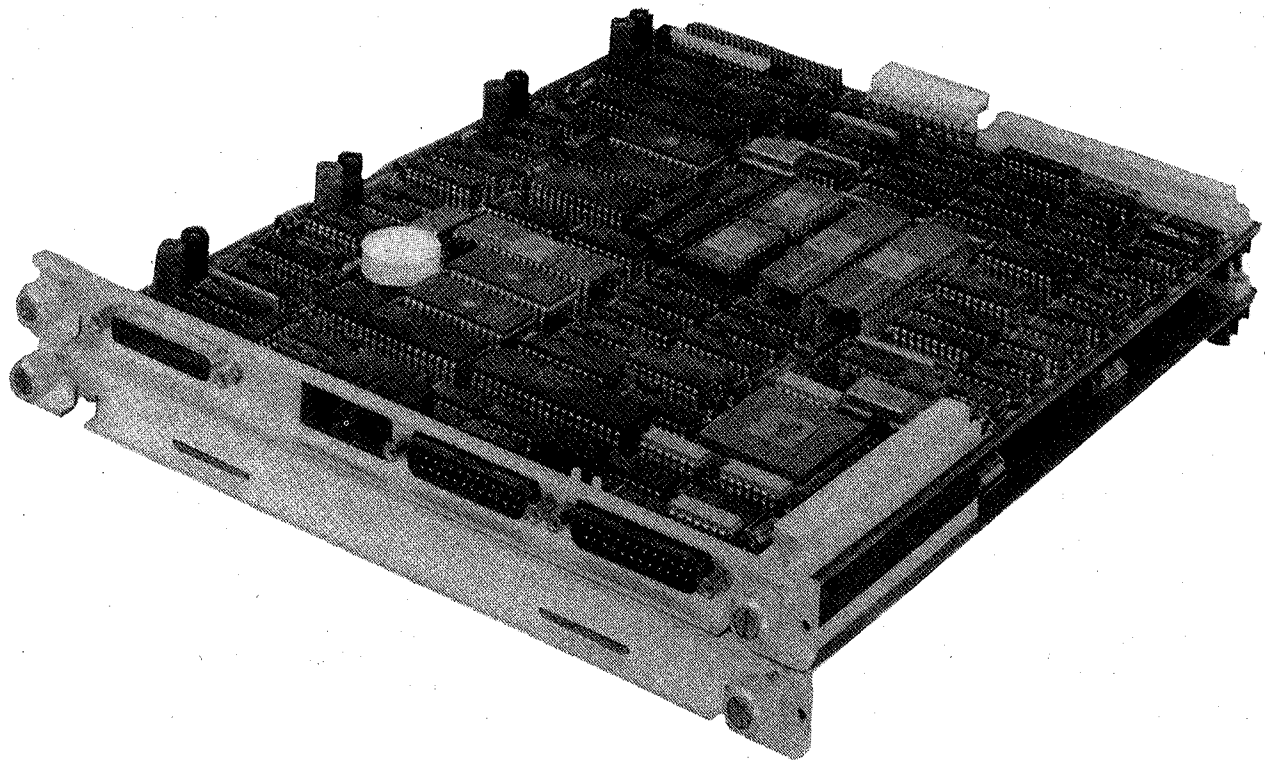
The operating system and MMU exchange information on the status of the memory pages through a Page Table in physical memory and the protection level on that page. By manipulating the Page Tables, an operating system dynamically controls the mapping of virtual to physical addresses. In particular, the operating system may specify that references to certain pages should generate translation error aborts. This mechanism implements virtual memory management and protection.

The MMU has an internal memory called the Translation Buffer, which contains direct virtual-to-physical address mappings of the 32 most recently used pages. Entries in the Translation Buffer are allocated and replaced by the MMU. The programmer is not involved in the process. The Translation Buffer is a content-addressable memory. The virtual page frame number (the 15 high order bits of the virtual address) and the address space bit are compared to the entries in the buffer. If the virtual page frame number is present in the buffer, the mapped physical address is output immediately. This is the case approximately 98% of the time, so most address translations take only one additional clock cycle. When the virtual page frame number is not present in the buffer, a control line is set, indicating to the control block that the memory page tables should be referenced. When this occurs, the MMU gets the corresponding mapping from memory and replaces the least recently used entry in the Translation Buffer with the new mapping.

NS32081 FPU (Floating Point Unit)

The NS32081 Floating Point Unit implements the most commonly used floating point functions in hardware to yield a great increase in speed over the software routines which it replaces. For example, a multiply routine in software requires approximately 1500 microseconds to execute. With the FPU, that time is reduced to approximately five microseconds.

The Floating Point Unit functions as a slave processor to the NS32016 (or any other Series 32000 CPU). Its high speed instruction set is consistent with the full two-address architecture and powerful addressing modes of the Series 32000 microprocessor family.



Functional Description (Continued)

The NS32081 FPU operates on two floating-point data types: single precision (32-bits) and double precision (64-bits). In addition, the FPU performs conversions between integer and floating-point data types. Integers are accepted and generated by the FPU as two's-complement values of byte (8-bit), word (16-bit) or double word (32-bit) in length.

Arithmetic operations include Add, Subtract, Multiply, Divide and Compare. Several Move and Convert instructions are also included.

NS32202 ICU (Interrupt Control Unit)

The NS32202 ICU is the interrupt controller for the Series 32000 microprocessor family. The ICM-3216 uses the ICU in the eight bit mode which allows for up to 16 hardware interrupts with programmable priorities. Four lines are used with the serial ports, one with the MiniBus controller, one with the SCSI port, one with the printer, and one with the real time clock. The remaining eight lines are available for use by the programmer.

Serial Communications

Two 2681 Dual Asynchronous Receiver/Transmitters provide four independent, full duplex, asynchronous receiver/transmitter channels with software selectable baud rates to 19.2 Kbaud. Two of these channels use the DB25 connector and implement the full set of RS232 signals:

- Tx Data
- Rx Data
- Request to Send
- Clear to Send
- Data Set Ready
- Data Terminal Ready
- Carrier Detect

The remaining RS232 channels use six wire modular telephone jacks, which are suitable for use with most terminals, and implement the following signals:

- I__SEND__DATA
- U__SEND__DATA
- I__MAY__SEND
- U__MAY__SEND

Parallel Printer Port/Input Port

One parallel port is provided. Direction of the port is software configurable. The CPU controls operation by accessing the parallel port command, status and data registers. The system is shipped with the port configured as a parallel Centronics printer port designed to operate with the IBM PC type printer cable.

Time of Day Clock with Calendar

The ICM-3216 Time of Day Clock with Calendar uses the MM58274 Real Time Clock/Calendar chip. It functionally consists of 13 4-bit binary coded decimal (BCD) counters ranging from tenths of seconds to tens of years, plus a day of the week counter. These counters are updated synchronously every tenth of a second. Leap years are automatically registered. Time can be programmed for the 12 hour mode (with AM and PM) or the 24 hour mode. Clock/Calendar Addressing is shown in the following table.

Clock/Calendar Addressing

Address	Read or Write	Function
A00000	READ	Control register status
	WRITE	Control register command
A00002	READ,WRITE	Seconds-tenths
A00004	READ,WRITE	Seconds-units
A00006	READ,WRITE	Seconds-tens
A00008	READ,WRITE	Minutes-units
A0000A	READ,WRITE	Minutes-tens
A0000C	READ,WRITE	Hours-units
A0000E	READ,WRITE	Hours-tens
A00010	READ,WRITE	Days-units
A00012	READ,WRITE	Days-tens
A00014	READ,WRITE	Months-units
A00016	READ,WRITE	Months-tens
A00018	READ,WRITE	Years-units
A0001A	READ,WRITE	Years-tens
A0001C	READ,WRITE	Day of week
A0001E	READ,WRITE	Clock setting register

The clock/calendar circuitry has battery back-up to keep the time current when no external power is supplied.

Small Computer System Interface (SCSI)

The Small Computer System Interface (SCSI) is an Intelligent Peripheral Standard defined by the American National Standard Institute (ANSI). SCSI is derived from the Shugart Associates Standard Interface (SASI), which is based on the IBM I/O channel. ANSI has defined Command/Status Sets for five types of I/O devices:

Random Access—	Rigid and Flexible Disk
Sequential Access—	Start/Stop and Streamer Tape
Write Only Devices—	Printers and Plotters
Processor Devices—	Host to Host Communications via SCSI
Network Devices—	Host to Host Communications via LAN

The use of the ANSI Standard reduces the system integration time by providing plug compatibility and command standards for the peripherals and allowing utilization of existing I/O drivers.

ICM-3216 uses SCSI to control the interface to rigid disk and to streamer tape. SCSI is controlled by an I/O channel controller supporting the full asynchronous SCSI protocol, including arbitration and reconnection. The interface operates only as an initiator on the bus; the peripherals connected to the bus operate

Functional Description (Continued)

as targets. The interface is implemented using a Z80B microprocessor and an NCR 5385E SCSI device.

This controller handles the physical path management between the NS32016 (host) and the target disk or tape device including arbitration, selection, disconnection and reconnection. The operation starts when the host NS32016 places a command descriptor block (as defined by SCSI) in memory. The I/O channel controller acquires the SCSI bus during the arbitration and selection phase, supplies the command to the selected target, manages the transfer and interrupts the CPU when the target issues the command complete message. The I/O channel controller does no interpretation of the commands or data transmitted between the host and the target; it only manages the transfer. The full power of the SCSI command structure is available to the host without the host suffering the overhead of the SCSI physical path management.

The SCSI can be connected to as many as seven target controllers, each of which can control up to eight devices. Up to eight devices may be operated concurrently. This permits overlapping disk operations for read, write, seek, etc.

The I/O channel controller is initialized by I/O commands. Subchannel target commands are controlled by I/O Control Blocks (IOCB) in main memory. Once the host sets up the command in memory, the I/O channel completes the command and interrupts the host. The host then examines the IOCB(s) to check for errors or for proper completion.

Data transaction between dynamic RAM and a target are accomplished with direct memory access of 16-bit word transfers. This provides 1.5 Mbyte per second (full SCSI bandwidth) transfer in or out of dynamic RAM while still permitting the CPU access to the dynamic RAM an average of 50% of the time during target transfers.

MiniBus

MiniBus is a high performance, synchronous 16-bit bus with full support for multiprocessors, complete with parity on address and data lines and physical addressing of all MiniBus masters (8 maximum). The MiniBus interface is provided through the MiniBus Interface Controller (MBIC). This single CMOS LSI compatible component attaches directly to the NS32016 bus and provides the complete bus interface.

MiniBus is not designed to compete with any of the 32-bit buses whose purpose is to satisfy the bandwidth requirements of multiple 32-bit processors. Rather, it is intended to provide a low cost, low power, low real estate bus with similar multiprocessor system characteristics on a smaller scale (16 bits of data, 8 masters).

Virtually all the LSI peripheral chips to support LAN's disks, terminals, floppies, tapes, GPIB and other system requirements are designed in 8- or 16-bit widths and are cheaper and more convenient to implement on a 16-bit bus when bandwidth permits. MiniBus is designed for these types of applications and provides very cost effective solutions in these situations. The MBIC is available to the customer for design of custom boards.

Memory

The ICM-3216 memory board contains the dynamic RAM for the ICM-3216 Integrated Computer Module. This board is populated with 144 RAM devices organized in an 18-bit wide data bus which allows for 16 bits of data plus byte parity. The board is designed to accept either 64k or 256k 150 ns dynamic RAM devices which operate with the Series 32000 CPU cluster at 10 MHz with no wait states for RAM access. Each board can contain up to 1 Mbyte of memory with 64k RAMs and up to 4 Mbytes of memory with 256k RAMs installed. The system design permits a maximum of two memory boards, each containing the same RAM device type, allowing 1, 2, 4 or 8 Mbyte systems to be configured.

Interface between the CPU board and memory board(s) is provided by two connectors. The MiniBus connector is not used on the memory boards except to provide structural stability for the Integrated Computer Module. The memory port is proprietary and is designed to enhance NS32016 operation with the Integrated Computer Module and contains all necessary address, data, control and timing signals to provide this optimized operation.

Two EPROM sockets are provided on the CPU board. These sockets can be configured for a single pair of 2764, 27128, 27256 or 27512 devices for 16 Kbytes to 128 Kbytes of ROM memory space. When operating with System V/Series 32000, the boot EPROM provided begins at address location 00 on power up or reset and remains in this location until the first time address bit A23 is set to 1. At this time, this EPROM address is changed to start at address 800000H. The boot EPROM contains the initialization program that executes upon power-up or reset and a stand-alone ROM Monitor for ICM-3216. The following functions are provided:

- Display the sign-on message upon power-up or reset
- Perform on-board diagnostics

Initialization

Upon power-up, the following ICM-3216 parameters are initialized:

The console channel baud rate is set to 9600 baud.

The character structure is set to 1 stop bit and 8-bits, no parity.

A unique value is written into all 1 Mbyte increments, then read back again. Addresses wrap around if the system is less than fully configured.

Functional Description (Continued)

The MiniBus Interface Controller is initialized by unlocking the interrupt circuitry so that a power fail or Bus Conflict NMI can get through.

The Memory Management Unit, Floating Point Unit, Interrupt Control Unit, MiniBus Interface Controller registers and the parallel port are initialized.

Power On Confidence Checks

Various power-on confidence checks are performed to insure that certain basic functions of ICM-3216 are working correctly. Memory and the parity circuits are tested as follows:

Parity Circuit: Data with even parity is written out and then read back with odd parity. A check is made for a Non-Maskable Interrupt (NMI) due to parity errors. This test is performed for two different bytes to insure that the correct byte and appropriate RAM is indicated.

Memory: A hexadecimal pattern is written to all memory locations. It is then read back, checking for parity errors. The system cleans up by writing zeros to all memory locations.

- Format Disk

  This allows a user to format a raw disk for use with the system. The disk must previously have been connected to the SCSI channel. The user then follows a menu to supply format parameters.

- Load Disk from Tape Drive

  System V/Series 32000 is supplied to the user on a 30 Mbyte (450 ft) tape cartridge. The user copies from tape to disk using the monitor's copy command. The ICM-3216 system must be configured with a console, a disk drive and a tape drive. At least 28 Mbytes of disk space is required.

- Execute the Monitor Program

  The monitor operates in one of two modes, controlled by a software switch:

  User Mode: the monitor reads command inputs from a terminal and executes the command with a Line Feed (<LF>).

  System Mode: input may come from a terminal as above or from a program generating command strings. This mode is meant to be used by programs sending commands to the monitor without human intervention.

  Monitor commands include Download Memory, Examine Memory, Modify Memory, Print Registers, Change Registers, Write Pattern, Set Breakpoint, Test Memory, Display Memory Size, Single Step and GO.

- Enter Operating System

After the system has completed the power on or reset sequence, it comes up in the monitor mode. After System V/Series 32000 has been installed, the monitor command B <cr> will cause the operating system to boot.

Operating System

ICM-3216 uses System V/Series 32000, a validated version of AT&T's UNIX System V. System V/Series 32000 is a powerful, multi-tasking, multi-user operating system with the following key features:

- Demand Paged Virtual Memory
- Hierarcical file system
- Source Code Control System (SCCS)
- UNIX to UNIX copy (uucp)
- Record and File Locking and High Level Language Programming
- C, FORTRAN 77 and (optional) Pascal compilers

Reconfigurable binary drivers are available for the following:

- SCSI using the EMULEX disk controller model MD01.
- SCSI using the EMULEX tape controller model MT02.
- 4 RS232C serial ports.
- Parallel Printer port.

This operating system is available on streamer tape as an unbundled binary system. The source for the above drivers is provided for use as examples for those wishing to generate their own drivers. A binary license and distribution agreement is required.

Specifications

Physical

Width:	11.02 in. (280 mm)
Height:	9.18 in. (233 mm)
Depth:	0.80 in. (20 mm)
Weight:	
CPU Board:	26 oz.
Memory Board:	24 oz.

Operating temperature:	0°C to +55°C (+32°F to +131°F)
Storage Temperature:	−30°C to +55°C (−22°F to +131°F)
Relative Humidity:	0 to 90%, noncondensing

Power Requirements

	+5VDC±5%		+12VDC±5%	−12VDC±5%
	Typ	Max	Typ	Typ
CPU Board	5.2A	6.2A	57 mA	57 mA
1 MB Mem Bd	1,25A	1.5A	—	—
2 MB Mem Bd	1.0A	1.2A	—	—
4 MB Mem Bd	1.25A	1.5A	—	—

SPECIFICATIONS (continued)

Connectors

Board/ Connector	# of Pins	Function	Connector Type	Mating Connector
CPU J1*	96	MiniBus	Direct Connect	Direct Connect
CPU J2*	96	Memory	Direct Connect	Direct Connect
CPU J3	10	PS Control	10-pos 0.156 ctr	AMP 1-641150-0
CPU J4	10	Reset/LED	10-pos 0.100 ctr	3M 3473-6000
CPU J5	50	SCSI	50-pos 0.100 ctr	3M 3435-6000
CPU P1	36	Printer	DB25 female	DB25 male
CPU P2	6	RS232	RJ19 6-wire s	RJ19 6-wire p
CPU P3	6	RS232	RJ19 6-wire s	RJ19 6-wire p
CPU P4	36	RS232	DB25 male	DB25 female
CPU P5	36	RS232	DB25 male	DB25 female
MEM J1*	96	MiniBus	Direct Connect	Direct Connect
MEM J2*	96	Memory	Direct Connect	Direct Connect
V1-V4	1	Power	Banana Plug	Banana Jack
G1-G4	1	Ground	Banana Plug	Banana Jack

The Direct Connect Fixtures consist of a 96-pin female DIN connector and a shroud to adjust spacing. The connector is attached to the board with the female side on the top. The pins from the bottom of the connector provide a male DIN connector which extends into the shroud. The boards then "stack" together using the MiniBus and Memory Direct Connects to electrically interconnect the boards.

EPROM Addressing

At power-up and after a power reset, the MSHADOW flip-flop is asserted. In this condition, EPROM can be read from a starting address of 0 or 800000H. The first CPU access with the most significant address bit (A23) set to 1 clears MSHADOW. At this time, EPROM is available only from a starting address of 800000H.

Memory Map

Address Range, Hex	Read or Write	Function
000000-01FFFF	READ, WRITE	Dynamic RAM, bootload EPROM
020000-7FFFFF	READ, WRITE	Dynamic RAM only
800000-81FFFF or 900000-91FFFF	READ	Bootload EPROM
A00000-A0001E	READ, WRITE	Clock/Calendar
A00020-A0003E	READ, WRITE	Serial Ports 1 and 2
A00040-A0005E	READ, WRITE	Serial Ports 3 and 4
A00080-A00082	READ, WRITE	Parallel Port
A000A0	READ	I/O channel status register
	WRITE	I/O channel command register
A000C0	READ	NMI status
	WRITE	MiniBus/Hold
A000C2-A000C8	WRITE	LED Array
A000CA	WRITE	LED MiniBus Reset
A000CC	WRITE	Even/odd parity select
A000CE	WRITE	Set parity enable
A000E0	READ	Enable NMI
	WRITE	Registers MHL and MCL
C00000-FDFFFF	READ, WRITE	MiniBus memory address 000000-3DFFFF
FE0000-FEFFFF	READ, WRITE	MiniBus 8-bit I/O access
FF0000-FF7FFF	READ, WRITE	MiniBus 16-bit I/O access
FFFE00-FFFFFF	READ, WRITE	Interrupt Control Unit

SPECIFICATIONS (continued)

Reliability

A comprehensive three phase testing program ensures that all products conform completely to specifications throughout their lifetime.

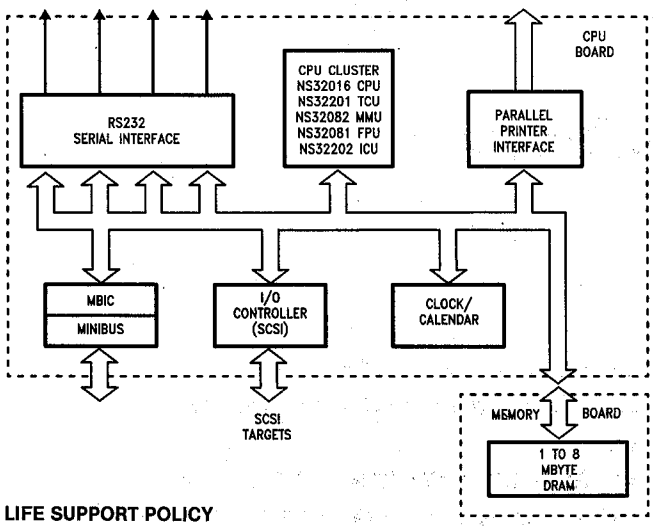
The first phase is an in-circuit test performed on the board after it is assembled. The circuitry on the board is exercised with a set of tests designed to uncover any manufacturing induced malfunctions.

The second phase is functional testing. The PCB is put in an oven and exercised at an elevated temperature with a full set of diagnostic programs. This phase is designed to eliminate infant mortality and to ensure board functionality over environmental as well as operational extremes.

The third phase is the system configuration test. The PCB is connected to a standard system and is tested with system level software. This test is designed to ensure the board's functionality in a system level environment.

The testing program ensures complete product functionality.

ICM-3216 Block Diagram



Ordering Information

ICM-3216	ICM-3216 CPU board with series 32000 CPU cluster (NS32016 CPU). Four RS232 serial ports, parallel port, SCSI interface and MiniBus.
ICM-3216-1MEM	ICM-3216 Memory board with 1 Mbyte of 150 ns DRAM.
ICM-3216-4MEM	ICM-3216 Memory board with 4 Mbytes of 150 ns DRAM.
ICM-3216-SYSV	System V/Series 32000, UNIX V.2.2 Operating System ported to ICM-3216 hardware.
ICM-CBL-TELCO	Cable, Telco, 6-wire, 7 ft.
ICM-CON-MAL	Adaptor, Telco to DB25 male connector
ICM-CON-FEM	Adaptor, Telco to DB25 female connector

Documentation

ICM-3216-M	ICM-3216 Hardware Reference Manual (420610289-001)
ICM-3216-SV-MS	UNIX V.2.2 Software Manual Set (970610289-001)
	ICM-3216 ROM Monitor User's Guide (424610289-001)
	ICM-3216 Device Driver Writer's Guide (424610288-001)
	ICM-3216 Administrator's Guide (424610287-001)
ICM-3216-MON-M	ICM-3216 Monitor User's Guide (424610289-001)

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