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ICM-3216 Memory Board Specification

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1. Introduction

The ICM-3216 Memory board contains the dynamic RAM for the ICM-3216 computer. The ICM-3216 is a complete computer system on two, double Eurocard size, printed circuit boards. All functions, such as CPU, memory, disk interface and I/O are contained on the ICM-3216 board set. The memory board will accept either 64K or 256K dynamic RAMs providing 1 to 4 megabytes of memory respectively. The system design will permit a maximum of two memory boards, each having the same RAM device types, to be installed at once. The other board is the CPU module which contains the NS32016 CPU cluster, boot EPROM, four serial interfaces, address mapping logic, SCSI interface, real-time clock, parallel printer interface and MiniBus interface. The CPU board is specified in document 426010289-000.

The ICM-3216 Memory board is designed to accept 150 nanosecond dynamic RAM devices and operate with a CPU board operating at 10 megahertz with no wait states for RAM access.

2. Features and Options

2.1. Features

The features of the ICM-3216 Memory board include:

- o 150 nanosecond RAM devices for 10 megahertz CPU board operation.
- o 144 RAM devices organized with 18 bit wide data bus.
- o Timing control for CAS and row / column addressing.
- o Control signal, address and data buffers.
- o Address decoding.

2.2. Options

The following options will be selectable:

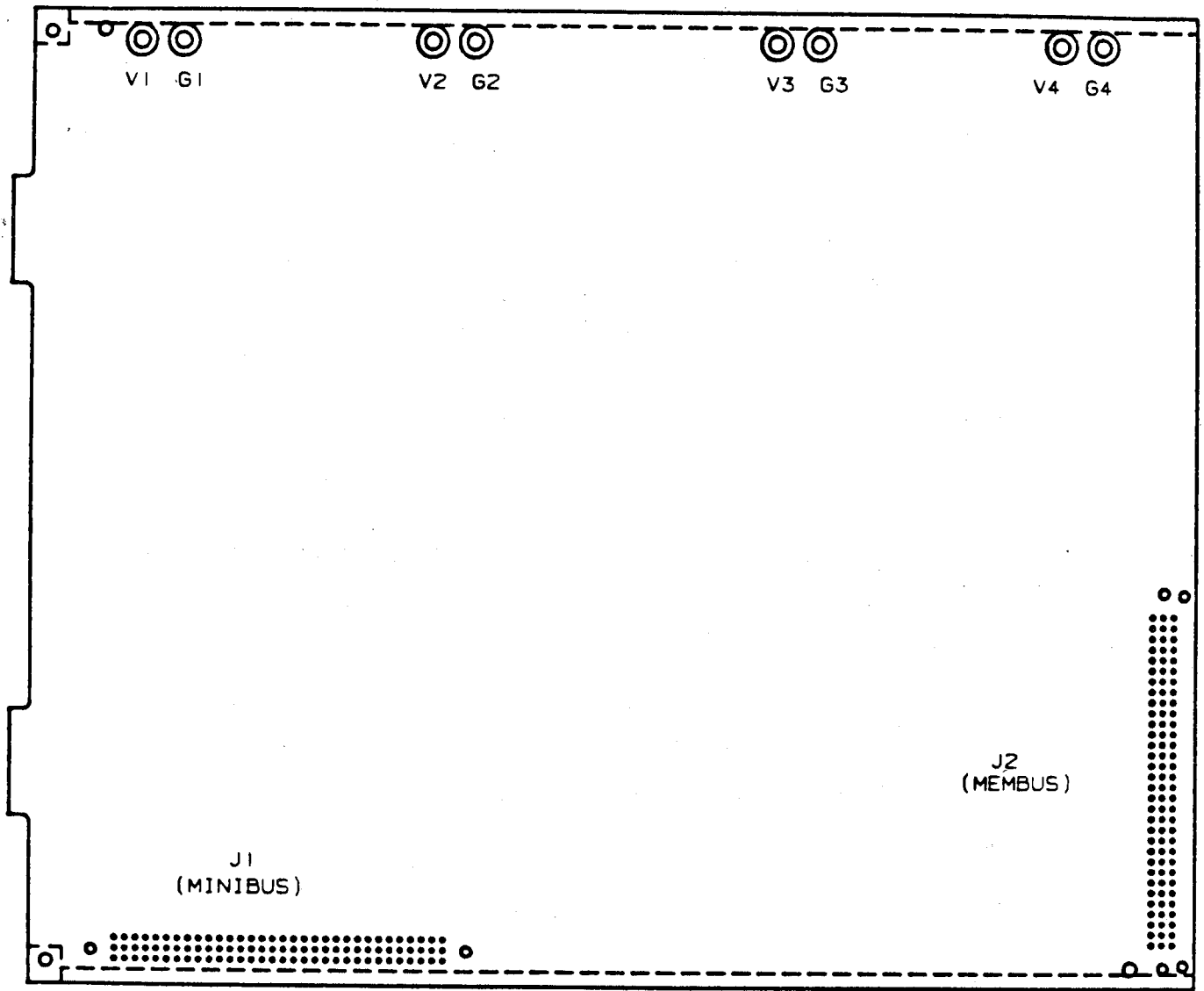
- o 64K or 256K RAM devices.
- o Selection of board 1 or board 2 in system.

3. Physical Description

The ICM-3216 Memory board is fabricated on a 11.020 inch by 9.180 inch printed circuit board (see Figure 1.)

Physical Characteristics:

Width:	11.020 in. (28.0 cm.)
Height:	9.180 in. (23.3 cm.)
Depth:	0.80 in. (2.0 cm.)



ICM-3216 MEMORY BOARD

4. Interface Pin Signal Lists and Descriptions

4.1. MemBus Interface - J2

Connector J2 connects the Memory board to the CPU board. Pin assignments for connector J2 are specified in Table 4.1.

MemBus Connector Pinout (J2)					
c01 -	gnd	b01 -	RAST	a01 -	gnd
c02 -	gnd	b02 -	gnd	a02 -	gnd
c03 -	MSHADOW	b03 -	RD~	a03 -	HLDD-RD
c04 -	HA2~	b04 -	HA3~	a04 -	A23
c05 -	HA0~	b05 -	+5V	a05 -	HA1~
c06 -	gnd	b06 -	+5V	a06 -	gnd
c07 -	WRMEML	b07 -	gnd	a07 -	WRMEMH
c08 -	gnd	b08 -	gnd	a08 -	gnd
c09 -	gnd	b09 -	CAST	a09 -	gnd
c10 -	gnd	b10 -	+5V	a10 -	gnd
c11 -	REFRESH~	b11 -	gnd	a11 -	gnd
c12 -	64K~	b12 -	RMA0	a12 -	gnd
c13 -	RMA1	b13 -	RMA2	a13 -	RMA3
c14 -	gnd	b14 -	+5V	a14 -	gnd
c15 -	RMA4	b15 -	RMA5	a15 -	RMA6
c16 -	RMA7	b16 -	gnd	a16 -	RMA8
c17 -	gnd	b17 -	AD00	a17 -	gnd
c18 -	AD01	b18 -	AD02	a18 -	AD03
c19 -	AD04	b19 -	gnd	a19 -	AD05
c20 -	AD06	b20 -	AD07	a20 -	AD08
c21 -	gnd	b21 -	AD09	a21 -	gnd
c22 -	AD10	b22 -	AD11	a22 -	AD12
c23 -	AD13	b23 -	gnd	a23 -	AD14
c24 -	AD15	b24 -	RDDP1	a24 -	RDDP0
c25 -	gnd	b25 -	WRDP1	a25 -	gnd
c26 -	WRDP0	b26 -	WRD00	a26 -	WRD01
c27 -	WRD02	b27 -	gnd	a27 -	WRD03
c28 -	WRD04	b28 -	WRD05	a28 -	WRD06
c29 -	gnd	b29 -	WRD07	a29 -	gnd
c30 -	WRD08	b30 -	WRD09	a30 -	WRD10
c31 -	WRD11	b31 -	gnd	a31 -	WRD12
c32 -	WRD13	b32 -	WRD14	a32 -	WRD15

Table 4.1

J2 - MemBus Pin Assignments

<u>MNEMONIC</u>	<u>SIGNAL DESCRIPTION</u>
AD15 - AD00	Read Data, bits 15 through 00. Data word read from RAM.
WRD15 - WRD00	Write Data, bits 15 through 00. Data word written to RAM.
RMA8 - RMA0	RAM Address, bits 8 through 0. Represents RAM row address or column address. RMA8 is used only with 256K RAMs.

RAST	Row Address Strobe. Indicates RMA8 - RMA0 is row address.
CAST	Column Address Strobe. Indicates RMA8 - RMA0 is column address.
WRMEMH	Write Memory High. Asserted when writing the high-order data byte to memory.
WRMEML	Write Memory Low. Asserted when writing the low-order data byte to memory.
REFRESH~	Refresh, active-low signal. Asserted during a refresh cycle.
MSHADOW	Memory Shadow. Generated by CPU board; set upon power-up, cleared upon memory access with A23 = 1. When set, prevents RAM access, allowing CPU board EPROM to occupy low address space.
HA0~ - HA3~	High-Order Address. Represents CPU address bits 17 through 20 when using 64K RAMs; bits 19 through 22 when using 128K RAMs.
A23	CPU Address 23. Must be low for RAM access.
64K~	64K RAM. A jumper-set low level indicates that the memory board uses 64K RAMs; a high level indicates 256K RAMs.
RD~	Read. Asserted when reading data from memory.
HLDD_RD~	Hold Data Read. Extends read data valid beyond RD~.
RDDP0, RDDP1	Read Parity. Low-order byte and high-order byte parity bits read from memory.
WRDP0, WRDP1	Write Parity. Low-order byte and high-order byte parity bits written to memory.

4.2. MiniBus Interface - J1

J1 is a MiniBus connector but is used only for power connection and mechanical rigidity of the multiple board assembly. The pin signal list of the connections made to J1 are shown in Table 4.2.

MiniBus Connector Pinout (J1)					
c01 -	gnd	b01 -		a01 -	gnd
c02 -		b02 -		a02 -	
c03 -		b03 -		a03 -	
c04 -		b04 -		a04 -	
c05 -		b05 -	gnd	a05 -	
c06 -	gnd	b06 -	gnd	a06 -	gnd
c07 -		b07 -	+5V	a07 -	
c08 -		b08 -	+5V	a08 -	
c09 -		b09 -	+5V	a09 -	
c10 -		b10 -	gnd	a10 -	
c11 -	gnd	b11 -	gnd	a11 -	gnd
c12 -		b12 -	+5V	a12 -	
c13 -		b13 -	+5V	a13 -	
c14 -		b14 -	+5V	a14 -	
c15 -		b15 -		a15 -	
c16 -		b16 -		a16 -	
c17 -	gnd	b17 -		a17 -	
c18 -		b18 -	gnd	a18 -	gnd
c19 -	gnd	b19 -	gnd	a19 -	gnd
c20 -		b20 -	gnd	a20 -	gnd
c21 -	gnd	b21 -	gnd	a21 -	gnd
c22 -		b22 -		a22 -	gnd
c23 -		b23 -		a23 -	
c24 -		b24 -		a24 -	
c25 -		b25 -		a25 -	
c26 -		b26 -	+5V	a26 -	
c27 -	gnd	b27 -	+5V	a27 -	gnd
c28 -		b28 -	gnd	a28 -	
c29 -		b29 -		a29 -	
c30 -		b30 -		a30 -	
c31 -		b31 -		a31 -	
c32 -	gnd	b32 -		a32 -	gnd

Table 4.2

J1 - MiniBus Pin Assignments

5. Environmental Requirements

Operating temperature: 0C to +55C

Relative Humidity: to 90%, noncondensing

6. Power Requirements

Power requirements for the ICM-3216 Memory board are as follows:

Board	Voltage	Tolerance	Maximum Current (amp.)
1 MB with 64K RAMs	+5V DC	+/- 5%	1.5
1 MB with 256K RAMs	+5V DC	+/- 5%	1.1
2 MB	+5V DC	+/- 5%	1.2
4 MB	+5V DC	+/- 5%	1.5