National Semiconductor

PRELIMINARY
March 1992

NS32SF641-16/32, NS32SF641-20/40, NS32SF641-25/50*
NS32SF640-16/32, NS32SF640-20/40, NS32SF640-25/50
Superscalar 64-Bit Integrated System Processor

General Description

The NS32SF641 and the NS32SF640 are highly-integrated, superscalar, RISC microprocessors. They are members of the Series 32000®/EP family of National Semiconductor's Embedded System Processors™ which are designed especially for computation-intensive, embedded applications. The NS32SF641 and the NS32SF640 are software compatible with other microprocessors in the same family. In addition, they provide new features which support graphics and Digital Signal Processing (DSP).

Unless otherwise specified, every reference to the NS32F641 in this document is applicable to the NS32F640 as well.

The NS32SF641 RISC CPU core incorporates two integer units, each of which has a five stage pipeline, a floating-point unit with an array multiplier, and instruction and data caches. Its internal organization allows a high degree of parallel execution of instructions. A two channel DMA controller, a 15 level interrupt control unit (ICU), and a 16-bit timer are all integrated on the same chip with the CPU. This makes the device extremely attractive for cost-sensitive applications for which a high performance is required.

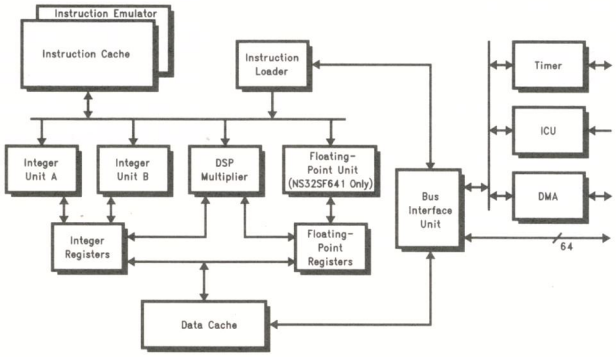
The system interface is also optimized to support many applications, including a wide range of highly sophisticated, embedded systems. The NS32SF641 integrates more than 1,000,000 transistors which are produced using sub-micron, double-metal, CMOS technology. The advanced level of its technology, combined with its mainframe-like design enable the NS32SSF641 to process up to 100 million instructions per second.

*In NS32SSF641-x/y,
x = bus clock frequency in MHz
y = internal clock frequency in MHz

Features

- Parallel instruction execution
- Software compatibility with the National Semiconductor Series 32000/EP family
- 4-GByte uniform address space
- Two integer units
- On-chip, single and double-precision, IEEE-754 compatible, floating-point unit (NS32SF641 only)
- Single and double-precision, IEEE-754 compatible, floating-point support through software routines (NS32SF640)
- 4096 byte, on-chip, decoded instruction cache
- 1024 byte, on-chip, data cache
- Very efficient DSP support
  - — 32x32 to 32-bit integer multiply in 20 ns
  - — 16x16 to 32-bit integer multiply in 20 ns
  - — Support for calculations using complex numbers
- High-performance/low-cost bus
  - — 32-bit address bus
  - — 64-bit data bus with dynamic bus sizing to 8, 16 and 32 bits
  - — Pipelined or sequential address/data transfers
  - — Support for two-way interleaved memory
  - — Full- or half-frequency bus clocking
  - — Support for page-mode and static-column DRAM
  - — Idle states for slow peripherals
- On-chip peripherals
  - — 15-level Interrupt Control Unit
  - — Two-channel Direct Memory Access (DMA) controller
  - — 16-bit timer/counter
- Built-in self-test
- Shadow-mode operation for fault-tolerance
- In-system emulation (ISE) and software debugging support
- External cache support
  - — Multiprocessing support

Block Diagram



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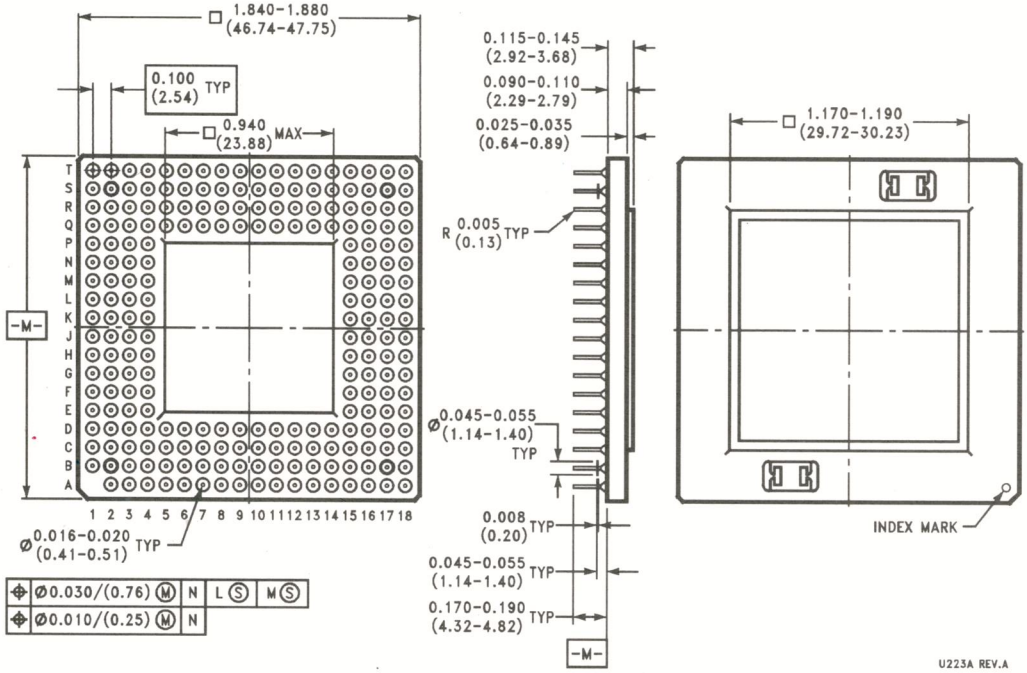
Superscalar 64-Bit Integrated System Processor

Physical Dimensions inches (millimeters)

Lit. # 114350



Ceramic Pin Grid Array (U)
Order Number NS32SF641U-16/32, NS32SF641U-20/40, NS32SF641U-25/50,
NS32SF640NU-16/32, NS32SF640NU-20/40, NS32SF640NU-25/50
NS Package Number U223A

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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