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National Semiconductor

Backgrounder

National Semiconductor's 100-MIPS Embedded Control Technology Combines 64-bit Architecture with Digital Signal Processing

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National Semiconductor's 100-MIPS Embedded Control Technology Combines 64-bit Architecture with Digital Signal Processing

A new generation of embedded processor technology disclosed by National Semiconductor Corporation achieves an unprecedented 100 MIPS performance through a 64-bit superscalar RISC architecture. In addition, the product offers high-performance, software-programmable digital signal processing (DSP) enhancements. This landmark technical achievement was developed by National Semiconductor's imaging technology team which was the first to offer an application specific embedded processor solution for imaging applications, and also the first to integrate DSP functions with a 32-bit processor to address the needs of the communications and multifunctional peripherals market.

With the newest addition -- called the Swordfish core, National Semiconductor's family of embedded processors covers the performance range from 1 to 100 MIPS. The 100-MIPS Swordfish core offers true superscalar performance, which means that its dual-pipelined integer execution units and the floating point unit can effectively execute two instructions per clock cycle. This is a significant enhancement of the inherent RISC capability of one instruction per clock cycle. The Swordfish core also features on-chip data and instruction caches, fast parallel execution of integer and DSP functions, fast context switching, and shadow mode operation for increased reliability.

A LEADERSHIP HERITAGE IN EMBEDDED PROCESSING

Beginning with its 32CG16 core introduced in 1987, National Semiconductor Corporation was the first to offer an application specific embedded microprocessor to efficiently integrate major system control functions. The 32CG16 was an immediate success in the laser beam printer market, and National quickly extended its high-performance core architecture to a series of advanced 32-bit processors.

The 32GX32 core was announced in 1989 and further extended National Semiconductor's performance range in embedded processing.

In May 1990, National Semiconductor announced three new imaging processors, including two (the 32FX16 and the 32GX320) that are the first 32-bit processors to incorporate true, software-programmable DSP capability. by integrating a high-performance 32-bit microprocessor with DSP, National Semiconductor was able to break through traditional performance and cost barriers. The new products for conventional fax, voice, modem, and printer technologies also created a new market for multifunctional peripherals.

The core-based family of embedded processors now includes:

- CG core processors (1-3 MIPS): 32CG16, 32CG160, 32FX16
- GX core processors (7-15 MIPS): 32GX32, 32GX320
- Swordfish core (50-100 MIPS): (to be productized)

The CG core and GX core processors have attracted design wins and support from companies including Adobe, Alcatel, Bitstream, Canon, CI Systems Design, Colorocs, Everez, Goldstar, GVC, HDE, Hewlett-Packard, Mannesmann Tally, Microsoft, Microdynamics, Microtek Labs, Mita, Phoenix Technologies, Samsung and TDS. In addition, widespread interest has been attracted for systems that integrate single-function peripherals such as fax machines, printers, scanners and terminals into one multifunctional system.

With this leadership well established, National Semiconductor is now disclosing the technology to extend performance for the next generation of computation-intensive embedded control applications.

MARKET GROWTH

The present range of National Semiconductor processors is successful in the market for current imaging processor designs requiring up to 20 MIPS performance. However, the forecast for market growth, according to both analysts and National Semiconductor, show that the market for 32-bit and 64-bit RISC embedded processors will grow nearly 10 times from 1.1 million units in 1990 to 10.9 million units in 1994. In this time period, 10 percent of this growth is expected to be in the high-end segment demanding performance in excess of 25 MIPS.

HIGH PERFORMANCE ACHIEVED

National Semiconductor's newest embedded processor technology disclosure combines a 64-bit processor with DSP and provides 100 MIPS capability. More than 1 million transistors are effectively connected into the Swordfish core. The Swordfish is the fastest superscalar technology with integer, DSP, floating-point, bus, and system functions. These combined features define the ultra-high-performance migration path for the next generation of embedded processors.

This new generation now under development at National Semiconductor utilizes 2 pipelines that enable the overall processing to proceed at two instructions per cycle. Thus, a 50-MHz core can deliver 100-MIPS processing speed.

The Swordfish surpasses the performance levels of today's most advanced host-type microprocessors. This performance leadership over host microprocessors marks a significant first for embedded processors.

ARCHITECTURE

Cast in the 0.8-micron version of National Semiconductor's M2CMOS process, the new core design will achieve its record performance levels via a true superscalar/RISC architecture that ensures simultaneous operation of its execution units over virtually the entire instruction set.

INTEGER UNITS

Integrating two independent integer units means that concurrently, in a single cycle, each of these units executes integer, control, or load/store instructions. Both integer execution units share the six-ported integer register file. In every clock cycle, this hexi-ported file permits the integer pipelines to read four operands and to write out two results. On-chip logic quickly and surely resolves data dependencies between concurrently executing instructions.

FLOATING POINT

The floating point unit performs single and double precision IEEE-754 floating point operations which include add, subtract, multiply, divide and various conversions between integer and floating point representations.

DSP

Multiply operations are the heart of DSP applications. The Swordfish integrates a fast array multiplier which greatly enhances performance in DSP operations. This Wallace-Tree array multiplier is shared by all execution units, allowing fast DSP in both integer and floating point domains. Integer multiply instructions of 32X32 bits execute in a single cycle. In addition, complex number calculations which are common in DSP, are supported by special, signed multiply instructions of 16X16 bits yielding 32-bit signed result. The functionality of these instructions allow the real and imaginary parts of a complex number to be stored in a single 32-bit register, thus significantly speeding up handling of complex numbers.

OPTIMIZING COMPILER

National's optimizing compiler was designed in parallel with the hardware it manages. Hence, the finely tuned hardware and software interact efficiently and quickly. This hardware/software integration is a key to effective RISC machine performance and ease of design.

National Semiconductor's 64-bit designs are superscalar RISC machines and their 32-bit relatives use ASIS (Application Specific Instruction Sets) -- and therefore contain complex instructions. The basic programming model of National Semiconductor's CG and GX cores has been scrupulously preserved in the Swordfish. Assembler translators will be available to migrate the software now in place.

ADDITIONAL FEATURES

The Swordfish bus can operate at 1/2 internal frequency (25 MHz) to promote ease of interface design and reduce system cost. Optionally the bus can run at a frequency equal to the internal frequency for maximum throughput. Dynamic bus sizing allows simple interface with 8, 16 and 32-bit I/O peripherals in the same system.

Fast, on-chip, 2-way set-associative data (1-kbyte) and instruction (4-kbyte) caches, in support of the Swordfish core also speed-up overall system operation. To further enhance system throughput, both caches are equipped with a locking mechanism that prevents the replacement of information deemed performance critical. On-chip Bus Snooping Logic ensures coherency between the data cache and main memory.

Moreover, integrating multiple processing units, caches, and system functions on the same chip eliminates the interface-transit delays of multi-chip solutions.

As part of its self-testing capability, the new core can be used in a "Shadow Mode." Here, one device operates as the master processor and the other as a redundant device that "shadows" the master. At each clock cycle the shadow processor monitors, and compares to its own, the outputs of the processor actually interfacing with the system. Upon a mismatch, the shadow indicates an error.

This same lockstep-operation provides pin-selectable program counter tracing capability to aid in debugging software. Here, 32 output pins of the monitoring device present the program counter contents for each cycle.

The 64-bit core also can rapidly switch from a currently-running task to another, and back again. This fast context switching capability, plus the ability to complete each task in record time, is the heart of real-time applications. Via an on-chip interrupt control unit, multiple-level interrupt handling and scheduling supports asynchronous events to complete the low-latency multi-tasking operation.

Practical embedded systems--with cost, power, and space constrains--will most often populate the uniformly addressed 4-GByte memory space offered by the 64-bit core design with relatively slow-acting DRAMs and EPROMs. With the resulting processor and memory cycle-time discrepancies in mind, National Semiconductor's designers are tuning the architecture to support interleaved memory to extend memory bandwidth.

HIGH PERFORMANCE MARKET

The fast-developing disciplines of data compression and decompression, pattern recognition and digital high-definition visual presentation are examples of how equipment designers will utilize this added processing power to meet increasing user expectations. Potential market segments for system implementations include advanced office peripherals such as high-end printers and print servers. These printers will be high resolution, PostScript, high speed, and/or color. Digital copiers and high performance color fax are also in this segment.

The performance of Swordfish enables the combination of these functions into one high-speed multifunctional device that may include voice and modem capabilities as well.

Robotics and machine tools, real-time data compression for mass storage voice compression, and voice and video compression in areas such as multimedia and interactive data bases make up the additional application areas.