MG-1 Main Board Hardware Description

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ABSTRACT

This document attempts to describe the current MG-1 hardware (Issue C). It is assumed that the reader has a copy of the Issue C Circuit Diagrams.

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1. Systems Overview

The main board can be conveniently divided into four main functional blocks (see Fig 1):

- The Processing Block containing the CPU & support, the DMA Controllers, interfaces to Ethernet, Hard & Floppy Disks, RS232 etc.
- The Video Block which is responsible for generating the 1024 x 800 pixel monochrome display of the MG-1, and includes circuitry to generate the system's Hardware Cursor. It takes its data directly out of the System DRAM using a 64-bit wide data path to reduce the rate at which accesses are required. It is also responsible for refreshing the System DRAM. The purpose of the Video Mapping RAM will be explained later.
- The DRAM System contains the memory chips, and the control, timing, & drive circuitry for upto 8Mbytes of DRAM. The DRAM is dual-ported between the Central Processing Block, and the Video Block allowing the processor to quickly & easily update the screen.
- The I/O Processor The system features a separate I/O Processor, whose purpose in life is to look after the keyboard, mouse, cursor, & buzzer. Thus when the mouse moves, the IOP can program the Video Block to place the cursor at a different location on the screen, or, if necessary, change the cursor shape - all without the intervention of the main processor.

  The IOP communicates with the main processor via an area of dual-ported RAM in the I/O Processor chip itself.

The next section describes in detail the contents of the four blocks mentioned above. The reader should refer to Fig 2 at this stage.

Note: To avoid cluttering the diagram too much, the 'Memory Request Control', 'Bus Arbitration', and 'Address Decode' blocks have been separated out on the right hand side of the diagram.

2. The Processing Block

The Processing Block consists of 24 functional blocks (including the J3 connector), joined together by four buses.

2.1. The Processor Block Buses

- LPB & PB - the Local Processor Bus, and the (buffered) Processor Bus are the main system buses. Both are 24-bits wide, with the lower 16-bits being Multiplexed Address & Data, and the upper 8-bits being address bits 16-23. PB is the buffered version of LPB, and contains indentical information, except during DMA operations (see later).

^ LLA ^ this bus contains the latched addresses from LPB0-15. (Since LPB16-23 always contain addresses, there is no need for these signals to be latched.)

^ MPB ^ the MOS Peripheral Bus is an 8-bit buffered bus, containing bits PB0-7, and is used to interface to the data buses of the 8-bit peripherals used by the system. It is used because the MOS periherals would not be able to drive PB sufficiently.

2.2. Address Decoding (Sheet 5)

Figure 3 shows the MG-1 Memory Map once the system has performed its initial power-on tests.

The MG-1 Memory Map is divided into 16 1MByte 'pages'.

The 1st two pages contain the on board DRAM (2Mbyte). There is room in the Memory Map for a further 6MByte to be added.

Addresses 0x800000 to 0xbfffff are unused.

ROM-PAGE contains the PROM, SRAM & VIDEO MAPPING RAM -see Fig 4.

IO-PAGE contains everything else the CPU can address on the main board - see Fig 5.

IBM-ADAPTER - this space is reserved for the WCW IBM PC Motherboard. This device performs its own address decoding.

2.2.1. Detailed Circuit Operation

When DRAM-ON/ is asserted, any address with LPB23 = 0 (ie any address in the range 0x000000 to 0x7fffff) is decoded as SYSTEM-DRAM.

LPB23 and PB22 (qualified by DRAM-ON/) are OR'ed together to give the gate on U249 (AA438). This enables the decoder for addresses in the range 0xc00000 to 0xffffff.

PB20 & 21 decode one of the 4 pages (C, D, E, & F) in this block. Pages C & E (outputs Y0 & Y2) are AND'ed give ROM-PAGE/. Page D (output Y1) is not used (by the main board). Page F (output Y3) gives IO-PAGE/.

The other half of U249 (AA91) decodes ROM-PAGE into 4 16KByte blocks. (Address bits 16-19 are ignored.) Two of the blocks decode to give EPROM-CS/, using U250 (AA92).

The SRAMs are allocated 16KBytes of space.

The 4th 16K block is allocated to the Video-Mapping RAM, but is decoded using U271 (XX1) & U213 (AA83) so that this signal can become valid before BDBE/ is asserted.

U233 (AA440) causes any ROM access, except Video Mapping RAM accesses, to assert ROM-CYC/, which is used to slow the bus cycle - see Sheet 1.

IO-PAGE

The I/O decode is performed by U232 & U231, which provide 16 decodes of 512 Bytes each, using LLA9-11, with LLA12 enabling U232, and LLA12/ enabling U231.

LLA15 is also used as an enable.

2.2.2. The Memory Map at Power-Up

When the MG-1 is first powered-up, (or Reset), the DRAM is disabled (DRAM-ON/ is FALSE), and the upper 4MBytes of address space are mirrored to the other 3 4MByte blocks.

The reason for this is that the CPU begins executing code from address 0x000000 after reset, and therefore it is necessary to have ROM at this address.

2.3. Bus Master Arbitration (Sheet 26)

The main board has the 4 potential Bus Masters:

Priority	Bus Master
1	LANCE
2	General DMA Controller
3	Raster-Op DMA Controller
4	CPU/MMU

2.3.1. Basic Operation

When the LANCE, or either DMAC requests the bus, the CPU is asked to relinquish the bus. When it does so, the highest priority Bus Requester is given the bus.

When a Bus Master relinquishes the bus, a new Arbitration Decision is made, & a new Bus Master is selected.

2.3.2. Detailed Circuit Operation

Assuming that the CPU has control of the bus, then S0-2 of U171 will be low (selecting the I0 input), Z/ of U171 will be high, & HOLD will be low.

When a request for the bus is made (by raising BREQETH and/or BREQDISK and/or BREQRAS), the request is latched by U170.

This causes U17 to select an input (I1-7) depending on the value on S0-2. The inputs to U171 are arranged such that the highest priority request is allowed to assert Z/ (i.e. set it to zero).

This inhibits further RQ-CLK/s, and asserts HOLD. HOLD is masked with FLOAT/ to overcome a CPU bug, which dictates that HOLD must not be asserted when the CPU is floating the bus. The HOLD/ signal is taken to the CPU, which asserts HLDA/ (Hold Acknowledge) once it has completed its current bus cycle.

The O/P of U229 (AA822) now goes high, which causes U211 (AA766) to asserts BACKETH/ (Bus Acknowledge for Ethernet) if U170 indicates that the LANCE is requesting the bus.

Otherwise, U211 (AA774) asserts its O/P, and U229 (AA823 & AA824) asserts BACKDISK (if there is a disk request), or BACKRAS.

When the Bus Master wishes to relinquish the bus, it negates its Bus Request which sets Z/ on U171 to '1' (since S0-2 have not changed). This removes the Clear input to U210, and allows RQ-CLK/ to clock again.

U210 acts as a delay line, so that if a Bus Request is already pending, it is acknowledged before the CPU regains control of the bus.

U179 (AA2) & U201 (SP001) cause the DMA Request input to the Winchester DMA Channel to be removed if the LANCE requests the bus whilst the General DMAC has the bus. This causes the DMAC to give up the bus (eventually), allowing the LANCE to gain control.

Similarly, U169 (AA776-9) & U159 (SP056) were used to cause the Raster-Op DMAC to give up the bus if there was a request from the LANCE or General DMAC pending.

2.4. CPU/FPU/MMU/TCU Cluster (Sheet 1)

The system is based on the National Semiconductor Series 32000, and uses the NS32016 Central Processor Unit, the NS32081 Floating Point Unit, the NS32082 Memory Management Unit, and the NS32201 Timing Control Unit.

These are connected together in a fairly standard manner - see Nat Semi data book if necessary.

Points to note are:

^ The ADS/ input to the TCU is generated from PAV/ and HLDAO/ (from the MMU) - so that the TCU doesn't generate cycles when the CPU/MMU have relinquished the bus.

^ Wait-States - The TCU will insert wait-states into a bus cycle for several reasons such as if a slow internal peripheral has been selected (i.e IO-PAGE/, RTC-CS/, or ROM-CYC/), or if a device on J3 (usually the IBM PC Motherboard) needs to slow the bus cycle down using BWAIT/. FWAIT/ is used to slow the cycle down when a clash occurs between a video and a CPU access to DRAM - see later.

^ SYSTEM-RESET is synchronised in the TCU and passed to the MMU, which OR's it with its abort signal to the CPU.

2.5. DMA Controllers & DMA Register (Sheet 2)

Refering to the Fig 2, the MG-1 features 2 DMA controllers. These are AMD Am9516s which are powerful devices with a 24-bit address space, 2 independent DMA channels with a variety of modes, and the ability to automatically load in new command information. The current clock speed used is 5MHz (P2 allows the clock frequency to be changed to 4MHz).

2.5.1. The 'General' DMA Controller (U267)

Channel 1 of this device is dedicated to handling data to/from the hard disk controller. As the hard disk controller is an 8-bit device, the DMA controller must perform 'Byte-Word' & 'Word-Byte' funneling when servicing this device.

The DMA-Request & DMA-Acknowledge from Channel 2 , (DREQ2/ & DACK2/), are passed through a CD4052 (U176) Differential 4-Channel Multiplexer/Demultiplexer. This allows this pair of signals to be sent to 4 different source/destination pairs, depending on the A & B inputs:

Input		DMA Channel 2	
B	A	Request	Acknowledge
0	0	RQ3/	ACK3/
0	1	RQ2/	ACK2/
1	0	RQ1/	ACK1/
1	1	FLPRQ/	(Not Used)

RQ1-3/ & ACK1-3/ are passed to the J3 connector, for use by the IBM Motherboard, the Laser Printer, or some other device on J3.

FLPRQ/ is the floppy request line from the Floppy Disk Controller (this device does not require a DMA-acknowledge signal).

This system, of course, imposes the limitation that only one of these devices may be active at one time, but fortunately these devices tend to be used fairly infrequently.

A & B are supplied by the DMA-register (see below).

2.5.2. The Raster-Op DMA Controller (U267)

This DMAC is hard-wired into the (now abandoned) Raster-Op hardware. It is no longer used. Later revisions may not have the Raster-Op components fitted.

2.5.3. The DMA Register (U227)

This is a 6-bit register, consisting of a 74C174, which latches the data on LPB0-4 & LPB7 on the rising edge of (WR/ + DMA-REG-CS/), ie the CPU may write to this register by writing to the DMA-REG area.

The bits of the register have the following functions:

Register Bit	Function
LPB0	Input 'A' of Multiplexer/Demultiplexer (see above).
LPB1	Input 'B' of Multiplexer/Demultiplexer (see above).
LPB2	DRAM-ON - used to enable the DRAM after initial systems checks.
LPB3	Latched, but not used.
LPB4	Latched, but not used.
LPB5	Not latched.
LPB6	Not latched.
LPB7	MG-1 'OFF' switch - MUST always be ZERO!

2.5.4. Other Points to Note

^ Bus Control Signals: The DMACs provide (& use) different bus control signals from the 32000 Series (i.e. ALE, R/W-, & ZDS/ instead of PAV/, RD/, & WR/), so it is necessary to convert between them.

When the CPU is bus master, and it accesses the DMACs, U158 (AA19) and U262 (AA20) are used to generate ZDS/ & ZWR/ from the CPU signals RD/ & WR/. (When CPU is bus master, HLDA is low - enabling the 'LS244.)

When a DMAC is bus master, PAV/ is generated from ADS using U320 (AA707) & U330 (AA567). (DMA-HOLDA is high when a DMAC is bus master.) The other bus control signals are converted on Sheet 3.

^ Addressing the DMACs: The chip select for each DMAC is derived from DMA-CS/ and LLA2, using half of U316 (AA15). LLA1 is fed to the Pointer/Data (P/D-) inputs, thus each DMAC occupies 2 word locations.

The other half of U316 (AA16) is used to decode the interrupt acknowledge signals (INTACK/) from DMA-INTA-CS/ and LLA2. This is used to allow the CPU to acknowledge an interrupt from the 'General DMAC' (U267).

^ Wait States: U253 (AA669) is used to synchronise ANY-WAIT/ to the DMA-CLK/ to give DMA-WAIT/.

2.6. The Ethernet Interface (Sheet 3)

The MG-1 Ethernet Interface consists of U208, an AMD Am7990 Local Area Network Controller for Ethernet (LANCE), and U207, an AMD Am7992 Serial Interface Adapter (SIA) plus the necessary glue to make it work. Alternative part numbers (shown on cct diag) are MK68590, and MK3891 respectively.

The Lance chip is too complex to be described in detail here, however, very briefly, this is what it does:

The Operating System sets up buffers in memory - some reserved for data to be transmitted, the others reserved for incoming data.

When the Operating System wishes to send data to another machine via Ethernet, it first puts the data in the Transmit Buffer(s), and informs the Lance that data is to be sent by setting a bit in an area of memory reserved for Transmit Control.

The Lance polls this area of memory every 1.6ms to see there is data to be transmitted - if there is, it automatically reads it from memory using its on chip DMA controller, serialises it, and outputs it to the SIA in the form of a PACKET with appropriate control information.

When receiving a Packet, the Lance takes the serial data from the SIA, deserialises it, and checks to see if this data is actually intended for the Lance's MG-1 (every packet contains its own destination address, and all packets on the net are received by every Ethernet Controller). If the packet is not intended for this machine, it is ignored. If the packet is intended for this machine, the LANCE continues to input data from the SIA, and DMAs it into the Receive Buffer(s).

If, when transmitting a Packet, the LANCE detects a collision (i.e. someone else on the net trying to transmit at the same time), it will abort the current packet and try again later.

2.6.1. The Glue

When the Lance requires the bus, it asserts its HOLD/ pin (BREQETH/). The bus arbitration logic gives the Lance the bus by asserting BACKETH/ (i.e. its HLDA/ pin).

When the CPU addresses the Lance, the address decode circuitry asserts ETHER-CS/. The Lance also requires Register Address Port Select (ADR) which is taken from LLA1.

The LANCE uses ZWR/ & ZDS/, as derived on Sheet 2.

ZDS/, ETHER-CS/ and RDY/ (which acts as an output when the Lance is the bus-slave), are gated by U213 (AA49), U250 (AA50), & U272 (AA642) to give BWAIT/ - this holds the CPU bus cycle up until the Lance is READY. (The Lance is a very slow bus slave - typical delays from asserting DAS/, to RDY/ being asserted are 600ns & 1400ns depending on circumstances).

When the Lance is bus master, PAV/ is generated using ETH-ALE, inverted by U315, 'Negative-ANDed' with ETH-TDBE/ using U319 (SP002), & feeding this through U254 (BB77). This gating with ETH-TDBE/ was used for early revision chips.

ETHREAD/ is used to start a memory read as early as possible since memory reads are more time-critical than memory writes. It is derived using U190 (SP003) to gate ETH-ALE with ZWR/. Thus a memory read cycle begins as soon as ETH-ALE is negated. Whether or not this is needed with the current memory scheme is debateable.

HBE/, RD/, WR/ are reconstructed from ZBYTE/, ZDS/, ZWR/ & LLA0, using U228 (AA51), U263 (AA52 & AA53) & U262 (AA56), which is enabled whenever HLDA/ is asserted (i.e. the CPU/MMU have reinquished the bus).

7. PB Buffering, MPB Buffering, & LLA Latching (Sheet 4)

2.7.1. PB Buffering

U248, U280, U270, U269, U281 are the LPB - PB Buffers. U248 buffers LPB16-23 onto PB16-23 because LPB16-23 always contains the non-multiplexed upper 8 address bits.

The buffering of the lower 16 bits is handled differently for two reasons:

[1] Since LPB0-15 contains multiplexed address/data, the direction of these buffers must be LPB -> PB during Address-Time. During Data-Time, the direction of these buffers depends on the cycle (read or write), and the area of address space being addressed.

U263 (AA711) & U228 (AA67) produce a signal which is low during the Data-Time of any read cycle, at all other times it is high.

U134 (AA64) & U263 (AA643) mask this signal when the device being accessed is on LPB.

[2] The DMA Controllers expect the low byte of data on LPB8-15, and the HIGH byte on LPB0-7. So during the Data-Time of DMA operations, U280 & U270 are enabled (by U320 (AA72) & U307 (AA71)), otherwise U269 & U281 are used.

Note: BUS-OFF/ is a signal that was used by the Raster-Op hardware.

2.7.2. MPB Buffering

U282 is the MPB buffer. It is enabled during the Data-Time of a cycle accessing a device on MPB by U230 (AA65), U295 (AA76), and U289 (AA68). The direction is controlled by DATA-RD/.

2.7.3. LLA Latches

U279 & U268 are the LLA latches. They use PAV (from U215 (XX39)) as the enable signal.

2.8. PROM, SRAM (Sheet 5)

2.8.1. PROM (U291 & U292)

The System PROM (actually EPROMs are usually used) area consists of two chips in order to give the 16-bit word required by the 32016 CPU - U291 supplies the low-byte onto LPB0-7, U292 supplies the high-byte onto LPB8-15.

They are each given 14 address lines (LLA1-14), allowing each PROM to hold upto 16K bytes.

The chip enable input is derived from the address decode cct (see below).

The O/P from U291 is enabled whenever LLA0 (and CE/) is low. U292 is enabled when BHBE/ (Buffered High Byte Enable) (and CE/)is low.

2.8.2. SRAM (U289 & U290)

The SRAM is arranged in a similar manner to the PROM except that WR/ is used to indicate whether a Read or Write cycle is required.

U290 supplies the low-byte, U289 supplies the high-byte.

LLA1-11 supply the addresses, giving a 2KWord RAM space.

SRAM-CS/ is masked with LLA0 (low-byte) and BHBE/ (high-byte) to give CS1/ for each chip.

The contents of the RAM are not lost when main-board power is removed because of VBACKUP (from the batteries on the Power Distribution Board).

POWER-OK/ (chip enable) ensures that the RAM chips are deselected when the main-board powered down.

2.9. ICU, USART, and RTC (Sheet 6)

2.9.1. The ICU (Interrupt Controller Unit)

The ICU (NS32202) is the 5th member of the 32000 Series used on the main board. Its data bus is connected to MPB0-7. It occupies 32 word locations, using LLA1-5 as its addresses.

The rest of its connections are all standard data book stuff.

It is set-up to have 16 possible interrupt sources, of which 12 are used:

Interrupt Line	Signal Name	Signal Source
IR0		(Not Used)
IR1	UST-RX-INT/	USART when it has recieved a character
IR2	BUSINT2/	J3
IR3	WININT/	Hard Disk Controller
IR4	DMA2INT/	General DMA Controller
IR5	BUSINT3/	J3
IR6	ETHINT/	Ethernet Controller
IR7	BUSINT4/	J3
IR8	FLPINT/	Floppy Disk Controller
IR9	BUSINT5/	J3
IR10	IOPINT/	I/O Processor
IR11	UST-TX-INT/	USART when it has transmitted a character
IR12	BUSINT6/	J3
IR13-15		(Not Used)

The INT/ is taken directly to the CPU's maskable interrupt pin (Sheet 1).

2.9.2. The USART (Universal Synchronous/Asynchronous Receiver/Transmitter)

The USART (8251A) takes its data from MPB0-7. LLA1 is used to select its Command or Data registers.

The chip clock used is the 1MHz IOP clock (IOPE). The Rx & Tx clocks are normally taken from COUT on the ICU (via P3).

Standard line drivers/receivers are used (U313 & U314), however, the following signal names (not the signals!) have the wrong polarity - DTR/, RTS/, & DSR/.

2.9.3. The RTC (Real Time Clock)

The RTC keeps track of the time whilst the MG-1 is powered down. It takes its power from VBACKUP, & is clocked by a 32768Hz crystal.

U274 & U321 are used to ensure that the RTC is deselected while there is no power (ie POWER-OK is FALSE).

2.10. The Video Processor (Sheets 9, 10 & 11)

The MG-1 contains circuitry to perform 'Hardware Raster-Op' called the 'Video Processor'.

This circuitry is no longer used since it was found that it was more convenient (& quicker) to use an entirely software Raster-Op implementation.

Therefore, there is no point explaining how it all works!

Later revisions of the board may not have the Raster-Op components fitted.

Note: Sheet 9 contains the System CTC (as opposed to the IOP CTC) (U294). One of its 3 channels was dedicated to the Video Processor.

Channel 2, however is used to generate the signal IBM-EOP/ which simulates the timing of the EOP signal an 8237 DMA controller (as used on the IBM PC) gives out. This signal is used by the IBM PC Motherboard, and is necessary because the EOP signal from the MG-1 DMA Controller has different timing characteristics.

2.11. Hard Disk Controller & Data Handling (Sheets 18 & 19)

The MG-1 uses the uPD7261 Hard Disk Controller (U217) to provide an ST506 interface to various hard disks. It is interfaced to the rest of the system using MPB0-7, RD/, WR/,HDC-CS/, LLA1 & RESET.

It is clocked by a 10MHz clock derived from OSC3, U320 (AA687), & U274 (AA578).

Since this is an 8-bit device, the DMA Controller must perform Word-Byte & Byte-Word funnelling when transfering data to/from it.

U296 (AA541) divides the 10MHz clock by two to give CLK-5MHZ (which is used on Sheet 2 to clock the DMA Controllers).

U254 (AA602 & AA604) is used to delay the 10 MHz Winchester clock slightly.

U194 & U235 buffer the status & control signals to/from the HDC. The enable line to U235 is connected to POWERFAIL so that when the power voltage goes out of tolerance (ie normally during Power-Up or Power-Down), writing to the disk is inhibited.

WINRQ is the DMA request line taken to the General DMA Controller (Channel 1).

U181 (BB13) allows upto 4 different disk drives to be selected.

The connector P5 contains all the Input/Output signal from the HDC & was included to allow the main board to support SMD Drives. Unfortunately, the need to byte-word funnel data reduced the bandwidth of the system to such an extent that the data rates required by SMD Drive could not be supported. Therefore this connector is never used.

UPD-HEAD-SELECT3 is required when larger disks are used since they have more than 8 heads (the maximum allowed by the HDC). This means that disks that require 'reduced write current' can no longer be used.

2.11.1. Hard Disk Data Handling (Sheet 19)

U221, U223 (Delay Line) & U222 are used to allow the HDC to vary the relationship between the data clock & the data written to the disk. This allows the HDC to move bits written to the disk closer together or further apart. The Line-Driver, U220 (AA298), takes the Pre-Compensated data & drives MEM-WT-DATA & MEM-WT-DATA/.

When reading data from the disk, the Line-Receiver U199 (AA299) is used. The Data Recovery chip (U273) recovers the data & supplies it (R-DATA) to the HDC, along with WINI-CLK & SET-LOCK/. Various discrete passive components (R22-28, C148-155) are required to get it to work.

2.12. Floppy Disk Controller (Sheet 20)

The MG-1 floppy disk control logic is based on the WD1770 Floppy Disk Controller chip (U297). The FDC is an 8-bit device, and is connected to MPB0-7, LLA1-2, DATA-RD, FDC-CS/, ZDS/ & RESET.

U255 (AA311) provides the correct timing for the WD1770 CS/ input by masking FDC-CS/ with ZDS/.

OSC4 & U320 (AA743) are provide the 8MHz clock for the chip (CLK-8MHZ). U296 divideds this to give CLK-4MHZ (which is used on Sheet 2 to provide an alternative DMA Contoller clock).

The signals provided by the FDC are used directly by the Floppy Drive which is connected to J8. U277 & U322 are line drivers for various signals.

FLPRQ/ is taken to the DMA Multiplexer/Demultiplexer & thence to the General DMA Controller Channel 2.

2.12.1. The Floppy Control Register

This is a 5-bit Write-Only Register, which the CPU can access by writing to FDC-REG. U255 (AA609) masks FDC-REG-CS/ with WR/, causing the data on PB0-4 to be latched on the rising edge of WR/ with FDC-REG-CS/ asserted.

The bits are used as follows:

PB	Signal Name
0	FLP-HEAD-SELECT
1	SINGLE-DENSITY
2	FLP-IN-USE
3	FAULT-CODE-LED
4	UPD-HEAD-SELECT3

- FLP-HEAD-SELECT selects the Floppy Drive head to be used.
- If Bit 1 is low, the FDC operates in DOUBLE-DENSITY mode.
- FLP-IN-USE enables the LED on the floppy drive
- FAULT-CODE-LED controls the front panel LED.
- UPD-HEAD-SELECT3 is used on Sheet 18 to allow large disks (with upto 16 head) to be used.

2.13. The J3 Connector

This connector provides the general purpose method of hardware expansion for the MG-1. A document describing the signals present on the connector is available separately.

3. The Video Section

The heart of the Video Section is a 6845 CRT Controller (U245). This is programmed by the IOP to generate the basic timing signals & characteristics of the display such as 'characters' per line, lines per frame, etc.

Although the MG-1 screen consists of a 1024 x 800 bit mapped array, the CRTC regards it as consisting of 16 columns by 50 rows of characters, each 64 pixels wide & 16 pixels high - see Fig 6.

At the end of each line, the CRTC produces an HSYNC signal (CRT-HS), and allows 4 character times for Horizontal Flyback.

These are utilised by the MG-1 main board to provide 1 cycle to get cursor data, & 3 cycles to perform DRAM refresh.

With 3 refresh cycles every line (21.3us), all rows in the DRAMs are normally refreshed every 1.8ms - which is well within the maximum refresh period of 4ms allowed (during Vertical Flyback the situation is slightly different - see below).

The Video Mapping RAMS

As mentioned earlier the MG-1 uses the 32082 MMU, which converts the Virtual Addresses generated by the CPU to Physical Addresses which are the actual addresses of the data in memory. For the purposes of address translation, memory is divided into 512-byte pages.

As a consequence of the way the Operating System uses this, it is unlikely that the 100KBytes needed for the screen will appear in consecutive pages in physical memory. This creates a problem, as the CRTC only generates linear addresses.

To overcome this, Video Mapping RAMs are used to convert the 'Virtual Video Address' generated by the CRTC into a 'Physical Video Address'.

3.1. CRT Controller With Video Address Map (Sheet 24)

Fig 9, & 7 illustrate the sequence of events described in this & the following sections. In Fig 9, the circled numbers identify example Video Characters as they make their way through the system.

U245 is programmed by the IOP via IOPD0-7 etc.

The character clock for U245 is CRT-VBA5 which is derived by dividing the Pixel Clock by 64 (hence video chars are 64 pixels wide).

The CRTC generates a 16-bit address (which indicates the 'Virtual Address' of the Video Character required) from MA0-3 (the Column number), RA0-3 (the Pixel Row number of the current 6845 'Character' line), MA4-11 (the 6845 'Character' Row number).

Address Bits															
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
MA 0	MA 1	MA 2	MA 3	RA 0	RA 1	RA 2	RA 3	MA 4	MA 5	MA 6	MA 7	MA 8	MA 9	MA 10	MA 11

P1 is used to allow the arrangment of these bits to be changed for the colour machine, but in the monochrome system, they are linked straight through (apart from 25-26 which is left unlinked).

U243 & U261 allow these addresses onto VA0-5 & VMA6-15 when CRT-TIME/ is asserted.

VA0-5 contain the address of the 64-bit Video Character in the page.

VMA6-VMA15 are used as 'look-up' addresses for the Video Mapping RAMs which provide the Video Address (VA6-21) (ie the address of the page required in physical

memory).

During CURSOR-TIME/, U224 enables the Cursor Row Number (CR0-5) (which is the address of the 64-bit Video Character), and the Cursor Page Number (CR6-7), onto VA0-5 & VMA6-7. VMA8-15 are held high by the pull-ups.

Thus each cursor takes up one 512-byte page of memory & upto 4 different cursors can be selected by the IOP.

During CURSOR-TIME/, U300 (AA371) ensures that VMA16 is low, so that the mapping address is taken from the lower half of the Mapping RAMs. At all other times (except when SYSTEM-TIME/ is asserted) U255 (AA372) & U300 (AA371) ensure that VMA16 is high.

Obviously, the CPU must be able to access the Mapping RAMs. U242 & U239 latch the addresses at PAV time, and are enables onto VM6-15 during SYSTEM-TIME/. U238 & U240 allow data to be transfered in the appropriate direction.

U255 & U300 now allow the state of LLA11 to be passed onto VMA16 to allow the CPU to access all of the RAMs.

3.2. Video Address Latches, Refresh etc. (Sheet 25)

VA0-21 contain the System DRAM address of the Video Character required.

V-ADD-STROBE/ (inverted by U258 (AA706)) latches these addresses onto U236, U237, & U241 just before the start of the Video Character Time in which they are used.

On the falling edge of VBA5, a Video Cycle is requested (see Memory Arbitration - Sheet 13), & some period of time later (depending on memory usage by the rest of the system) a Video Cycle is started - indicated by VIDEO-CYCLE/ being asserted. This enables U241, giving UPPER-MADDR(0-4), which are used on Sheet 12.

U236 & U237, controlled by VIDEO-RAE/ & VIDEO-CAE/, multiplex the lower 16-bits to give U-MUX-MADR(0-7) (also used on Sheet 12).

OSC1 produces the basic 60MHz clock used by Video Section, which is buffered by U133 to give the 3 'indentical' signals DOT-CLOCK, VIDEO-CLK, & 60MHZ-CLK.

DOT-CLOCK is fed to U87 & U111 which form a 6-bit divider chain giving the basic Video Clocks VBA0-5. The reason for the use of U87 (74F109) rather than just cascading two 74F161s (as done on Issue B boards) is that that arrangement can't be guarenteed to work at 60MHz. Using the 'F109 means that there is only a slight violation of worst case conditions at 60MHz!

U205 is used to synchronise the signals generated by the CRTC to the O/P from the Video section, because to the 2 Video Cycle delay between the CRTC issueing a new address & the data from that address appearing at the O/P of the Video Section.

U198 (AA555) generates CURSOR-TIME/*, & U198 (AA556) generates RFSH-TIME/*. U218 normally passes these straight through giving CURSOR-TIME/ & RFSH-TIME/, however during Vertical Flyback, U256 (AA759) asserts CURSOR-MUX, which causes these two signals to be swapped round - generating a lot of CURSOR-TIME/'s. The reason for this is discussed in the Cursor Section.

Whilst CURSOR-MUX is asserted no Refresh Cycles are generated (i.e. for 20 line times - 427us), which means that the worst case time taken to refresh all rows of DRAM is 2.2ms.

The generation of CURSOR-MUX has been changed for use with MRC. On machines with this modification, CURSOR-MUX is only asserted while VSYNC/ is asserted (i.e. for 16 line times - 341us), which means that the worst case time taken to refresh all rows of DRAM is 2.15ms.

U203 is the 8-Bit Refresh Counter, which is incremented at the start of RFSH-TIME. U204 enables this onto VA0-7 during RFSH-TIME.

3.3. Memory Buffering & Video Output (Sheet 17)

A key feature of the MG-1 Architecture is the Double Buffering of the Video Data. At the end of a Video-Cycle, U250 (AA259) strobes U147, U112, U124, U113, U125, U115, U126, U114 which latch the 64-Bits of Video Data present on their inputs.

On the next CRT-VBA5 rising edge, bytes 1-7 of this data are transfered to the second set of latches (U135, U148, U136, U149, U138, U150, U137), and a new Video Cycle is requested.

The 8 bytes of Video Data are now enabled onto VB0-7 at 133ns intervals by U142. The data in U147 will be used with 133ns of the next Video Request, & there is no way that a memory cycle can finish that quickly, so there is no need to double buffer this byte.

This double buffering means that we can request a Video Cycle long before it is needed, & not care too much about when it is completed, since we know it will always be completed within 1.07us. This ensures that we keep the delay caused to the rest of the system by the Video Section to a minimum.

U159 (AA732) & U77 (AA733) control the loading of the Video Shift Register (U110 & U86) which shift the video data out (producing IMAGE-VIDEO).

DISP-EN is synchronised with the loading of the shift registers to give SYNC-DISP-EN.

SYNC-DISP-EN, CURSOR-VIDEO, & IMAGE-VIDEO are re-syncronised to VIDEO-CLK by U84 (AA511), U76 (AA512), & U76 (AA513) repectively. The outputs from these are mixed with CURSOR-OR-FN by U75, according to the following Truth Table:

SYNC-DISP-EN/	IMAGE-VIDEO	CURSOR-VIDEO	CURSOR-OR-FN	AND Y0	AND Y1	AND Y2	AND Y3	OUTPUT
0	0	0	0	0	0	0	0	1
0	1	0	0	0	1	0	0	0
0	0	1	0	0	0	0	1	0
0	1	1	0	0	0	0	0	1
0	0	0	1	0	0	0	0	1
0	1	0	1	0	1	0	0	0
0	0	1	1	0	0	0	1	0
0	1	1	1	0	0	1	0	0
1	x	x	x	1	x	x	x	0

Where Y0 = SYNC-DISP-EN/
Y1 = CURSOR-VIDEO/.IMAGE-VIDEO
Y2 = CURSOR-VIDEO.IMAGE-VIDEO.OR-FN
Y3 = CURSOR-VIDEO.IMAGE-VIDEO/

Thus, if CURSOR-OR-FN is low, the O/P is the inverted EX-OR of CURSOR-VIDEO & IMAGE-VIDEO. If CURSOR-OR-FN is high, the O/P is the NOR of the two signals.

The inverting action above ensures that a '1' in memory appears as a BLACK pixel on the screen, & a '0' produces a WHITE pixel.

The O/P is re-synchonised to VIDEO-CLK (by U84 (AA262)) to eliminate skew problems that might occur through U75.

U73 is the Video Line-Driver, producing the final Video O/P signal. R6 is a pull-up which improves the signal quality at high frequencies D11 & D12 protect the output

from voltage spikes travelling back down the video cable.

Also on this Page: The System Data Latches

U88-91 & U100-103 are the System-Cycle latches. These are 74LS373s (transparent latches) which allow the data through as early as possible.

U187 (AA515) enables the latches while CAS-TIME is asserted, & disables it at CLOSE-CYCLE/.

The appropriate latches are enabled onto PB0-15 by RBS(0-3)L & RBS(0-3)H.

3.4. The Cursor Logic (Sheets 7 & 8)

The MG-1 features a hardware cursor, which can be positioned anywhere on the screen.

The cursor consists of a 64 x 64 pixel image. This image can be OR'ed or EXOR'ed onto the background.

To position the cursor on the screen, 3 counters are needed - see Fig 6.

[1] To count the screen lines to the start of the cursor.

[2] To indicate the Video Character in which the cursor starts.

[3] To give the pixel offset within the Video Character to the start of the cursor.

Two stages are used to determine the horizontal positioning of the cursor because of the difficulties of clocking an 11-bit TTL counter at 60MHz!

Every CRT Horizontal Fly-Back time, the data for the next line of the cursor (1 line of cursor = 64 pixels = 8 bytes) is taken from the System DRAM and loaded into a small, high speed, TTL Cursor RAM.

3.4.1. Cursor Positioning

The vertical position of the cursor is controlled by 'COUT1' from the IOP CTC (U286 on Sheet 22).

This counter counts Video Characters from the end of VSYNC/. The reason why it is necessary to count characters rather than lines will be explained later.

The IOP software ensures that the count terminates during the horizontal fly-back by programming the counter with:

Count1 = Characters-per-line * YPOS + offset

where offset has been chosen so that COUT1 reaches its terminal count at the Video Character after the appropriate CURSOR-TIME.

When COUT1 reaches its terminal count, it clocks U200 (AA674) low indicating that a cursor is required on this line.

COUT2 is triggered every line, so it clocks U200 (AA675) indicating that we want the cursor to start in the current Video Char.

However, due to its 'D' input, U200 (AA675) only clocks a zero through when the ROW is correct too.

U108 (AA713) synchronises this to the falling edge of VBA5 using U188 (AA673).

This causes U107 & U131 to be removed from their normal 'Load' state, and causes U107 to be enabled.

These counters form the Horizontal Offset Counter. The IOP loads them with the 2's Complement of the start postion (within the current video char) of the cursor. (If the counter is loaded with zero, the offset is 64-pixels.)

The counters now count upward, using the Cursor-Clock (60MHz for monochrome systems). (U131) QC & QD are loaded with 0 & 1 respectively, which causes END-OF-CURSOR/ (should really be called NO-CURSOR/) to be asserted, indicating that no cursor is to be O/P at this stage.

When the lower 6-bits of this counter wrap-round to zero, (U131) QC goes high, negating END-OF-CURSOR/ (which is used by the video mixing cct on Sheet 17).

3.4.2. Cursor Serialisation

Bit QD of U107 & bits QA & QB of U131 are enabled through U144 to give CBA0-3 (Cursor Byte Addres), used by the Cursor RAMs.

The data from the Cursor RAMs is passed via the Inverting buffer U180 to the cursor shifters U109 & U85 and thence to CURSOR-VIDEO, & the Video Mixing Section.

Data is clocked out using CURSOR-CLK. U133 (BB79) and U108 (AA565) produce LOAD-TIME which controls the loading of the Cursor Shift Registers.

U107 & U131 keep counting until all 8 bytes are O/P, at which point, all 8-bits of the counter wrap round to zero, re-asserting END-OF-CURSOR/.

At this point, U131's R-CLK O/P pulses low for half a clock period (8.3ns - U200 is an 74F74 in later issues of the board) which, via U190 (AA115) sets the 'D' I/P of U108 high again. This high is clocked through on the next VBA5 falling edge, ready for the next line.

Note: Because LOAD-TIME occurs at the START of each byte of the cursor, the addresses being presented to the cursor RAMs (and thus the data being presented to the cursor shifters) at this point have not actually changed to the new value. Thus the 1st byte of data O/P is actually the last one in the RAMs, ie the order of bytes O/P is:

Byte of Cursor	0	1	2	3	4	5	6	7
Byte of Video Char	7	0	1	2	3	4	5	6

3.4.3. Loading the Cursor RAM

As mentioned previously, every horizontal flyback time, the Cursor RAMs are loaded with data for the next line.

A cursor line requires 64 pixels (8 bytes) which is conveniently the amount of data extracted from the System DRAM by one Video Cycle. Thus only one 'cursor-read' cycle is required per line - this cycle is indicated by the assertion of CURSOR-TIME/.

U225 (the CURSOR-ROW-COUNTER) is incremented on the falling edge of CURSOR-TIME/ to give the Cursor Row Number required for the line just coming up. The exception to this is the 1st line of the cursor, where the counter is held clear (indicating that line zero of the cursor is required) by U200 - the IOP programs its CTC so that COUT1 occurs AFTER the CURSOR-TIME/ of the 1st line.

The Cursor Row (CR0-5) (from U225) is combined with CR6-7 (these bits are used by the IOP to select one of the four cursor shapes available to it at any one time) to give the CURSOR-ADDRESS.

These are passed to the VIDEO MAPPING RAMs (Sheet 24) which converts this address to the physical address required by the System DRAM.

The Video circuitry acquires the data, and multiplexes it a byte-at-a-time onto VB0-7. Due to the double buffering (Sheet 17), the data requested at CURSOR-TIME/ is not available on VB0-7 until two VBA5 clock cycles later.

For this reason, U182 is used to delay (and also lengthen) CURSOR-TIME/ - see Fig 7. This signal is used to enable VBA3-5 onto CBA2-0, to give the WRITE-ADDRESS to the Cursor RAMs. The write strobe (CB-WE/) is generated using VBA2 and the Q/ output of U182 (AA677) & U195 (AA112).

When all 64 rows of the cursor have been displayed, the counter clocks its 'Bit 6' high, which (during non-display time, with DISP-EN/ high) will preset U200 (AA674), causing the counter to be cleared ... COMPLETING THE CURSOR DISPLAY SEQUENCE FOR THIS FRAME!

3.4.4. Bleeding the Cursor Off the Bottom of the Screen

This is straight forward, except that we need to ensure that the cursor has been 'finished' before the next frame starts (otherwise it would 'wrap-around' at the top of the screen!).

There are not enough 'Line-Times' in the VERTICAL FLY-BACK period to do this (64 lines would be necessary), so logic on sheet 25 (U256 & U218) causes a CURSOR-TIME/ to be generated every video cycle during vertical fly-back.

This is more than sufficient to do the job!

Note: If the board has the MRC Mods done to it, CURSOR-TIME/s are only generated while VSYNC/ is asserted - this is because of complications with getting the MRC cursor to work.

3.4.5. Bleeding the Cursor On from the Top of the Screen

To do this we must cause the 1st line of the cursor displayed to be a line other than line zero.

This is done by starting the cursor 'early'. As before, there are not enough 'Line-Times' from the trail edge of VSYNC/ to the Start-of-Display, so the IOP software uses the fact that it can move the 'position' of COUT1 'character-by-character', to position it (COUT1) the appropriate number of CURSOR-TIME/s back into the 'burst' of CURSOR-TIME/s that we have generated as described above.

Thus the IOP uses a different method to calculate the value programmed into the COUT1 counter when a -ve Y-coordinate for the cursor is required.

3.4.6. Cursor Bugs

Apart from the timing problem mentioned earlier associated with U200 appear to be two further cursor bugs:

[1] When the cursor is in the last Video Char of a display line, some spurious dots can be seen at the very right hand edge of the display.

This bug is due to a clash between the cursor display circuitry trying to display the cursor & the video circuitry trying to load the cursor RAM with the next line of cursor data.

The clash occurs because of the 8 pixel (1 byte) overlap caused by SYNC-DISP-EN - 8 pixels are displayed after the end of DISP-EN since the video shifters are loaded at the very end of the 'data-valid' time on VB.

[2] If the cursor is moved in, or through, an area just to the right of a Video Char boundary, a 'random' pixel can sometimes be seen (on some machines). This only occurs when the cursor is moving.

This bug is not fully understood at present, but appears to be due to some obscure timing problem associated with U107, U131 & U108.

Note: These bugs are acceptable (at present) and machines with these faults should not be failed.

3.4.7. Header P8

This header allows the cursor logic to be clocked by a frequency other than 60MHz. This is used for the colour versions of the MG-1.

3.4.8. Header P11

This header allows the Cursor Row to be generated differently than described above - this can be used to generate an 'interlaced' cursor.

3.4.9. The Low Cost Colour Connection (P12)

This is used to supply video data & control signals to the MG-1 colour board.

4. The DRAM System

The Main Board DRAM System uses 64·DRAM chips to give a 64K x 64-bit word array (using 64K x 1 DRAMs) (512KBytes) or a 256K x 64-bit array (using 256K x 1 DRAMs) (2MBytes). Expansion cards increase the height of this array to a maximum of 1024K x 64-bits (8MBytes). See Fig 8.

The array is 64-bits wide to allow the high video pixel rate (60MHz) to be supported with the relatively low Video Cycle rate of one cycle every 1.07us.

When the Processor Block performs a read, 64-bits are read and latched, and the appropriate bytes are enabled onto PB0-15. When the Processor Block performs a write, only the appropriate bytes are written.

Thus the system sees the DRAM as a 16-bit wide array.

4.1. Memory Arbitration (Sheet 13)

This section of the circuitry ensures that the Video Section & the Processor Section do not attempt to access the System DRAM at the same time, by arbitrating between them.

The rising edge of PAV clocks the 'Bus Request Latch', U105 (AA464). The rising edge of VBA5/ clocks the 'Video Request Latch', U105 (AA644).

4.1.1. Consider a CPU access:

The O/P of U105 (AA4643) going low allows U152 (XX37) to clock U128 (AA461) whose O/P is re-latched by U128 (AA460) to cure meta-stability problems.

If SYSTEM-DRAM is high (i.e. main memory is being accessed), U127 (AA468) clocks U161 (AA457), which asserts BUS-REQ (&MEM-REQ).

SYSTEM-DRAM is also latched at the end of PAV/ by U80 (AA459), so that if a Video-Cycle is pending, F-WAIT/ is asserted - holding up the CPU (or other Bus Master).

If a CPU request is made when a Video Cycle is in progress, the CPU is held up, (put into wait states), since U80 (AA458 & AA459) cause F-WAIT/ to be asserted. However, BUS-REQ is still asserted, so as soon as CLEAR-TIME is over, a new memory cycle is started (MEM-REQ stays active).

Due to the position in its bus cycle at which the CPU 'waits' (T3), F-WAIT/ cannot be removed immediately. Instead, it is removed during the memory cycle by END-OF-WAIT - See Fig 12.

4.1.2. Now Consider a Video Request:

U105 (AA644) is clocked high. This allows U127 (AA466) to clock U129 (AA109) high, (Pin 2 of AA466 is high since we have assumed there is no CPU request pending), whose O/P is re-latched by U129 (AA109) (to cure meta-stability problems), which asserts VIDEO-CYCLE. One MEM-CLK later, VIDEO-REQ (& MEM-REQ) is asserted.

At the end of the memory cycle, CLEAR-TIME is asserted, which, using U184 (AA763), U81 (AA114 & AA469) & U153 (AA789), clears the appropriate latches [U161 (AA457) & U80 (AA459) for a Bus Cycle or U129 (AA455 & AA109) for a Video Cycle].

If a Video-Cycle request is made when a CPU cycle is in progress, it is held up until the CPU cycle is completed by U127 (AA466) or U127 (AA467). (U105 (AA464) is cleared as soon as the CPU request has been latched by U108.)

4.1.3. Simultaneous CPU & Video Request

If the CPU & Video request a memory cycle at virtually the same time, an attempt is made to hold up the Video Cycle (which has a lower priority), at U127, (AA466). If that fails a Video Cycle is done & the CPU is held up.

4.1.4. Bug Fixes for DMA Controllers

U214 (AA453), U82 (AA788) & U77 are necessary to overcome an Am9516 bug. When it swaps from channel to channel (internally) or gives up the bus, the Am9516 issues a 'Redundant ALE' (ie it issues T1 of a bus cycle, & then either stops (if its giving up the bus) or carries on with a new bus cycle with a new T1).

Since the system generates PAV from ALE when the DMAC is bus master, a new memory cycle will have been started.

U214 (AA453) effectively delays PAV by half a DMA-CLK and inverts it. This then causes U82 (AA788) to assert WAIT-KILL/ (since DMA-DBE/ is not asserted when a

redundant ALE is issued) which removes the F-WAIT/ & BUS-REQ.

WAIT-KILL/ must be issued quickly when the DMAC gives up the bus so as to avoid interfering with the next bus cycle, so DMA-HOLDA is used to clear U214 (AA453) when the DMAC gives up the bus, clocking U82.

U77 is necessary since the DMA-DBE/ can be active well into the next bus cycle, & if U82 is clocked to soon it may 'see' the DMA-DBE/ from the previous cycle, & therefore not assert WAIT-KILL/. Therefore, U77 is used to delay by half a DMA-CLK (100ns).

4.2. Memory Timing (Sheet 14)

U159 (SP053) & U143 (SP011) act as a 'Memory-Cycle-Enable'.

On a Video-Cycle the memory cycle is enabled as soon as possible.

On an Ethernet read cycle, the cycle is started as soon as the addresses are valid using ETHREAD/.

On a CPU read cycle, the cycle can be started as soon as the memory arbitration is complete, so it is enabled with DDIN/.

DMA cycles are not started until ZDS/ to overcome the DMA Controller's redundant ALE bug.

When the cycle is enabled, and MEM-REQ is asserted, the cycle starts, propagating '1's down the 16-bit shift register (made up by U162 & U185) clock at 60MHz.

U153 (AA566) & U184 (AA495) clear the shift registers once the high level has propagated through all 16-bits.

P7A & P7B provide a means of varying the exact relationship of the memory timing signals.

The links used on P7A are 3-4, 5-6, 7-8, 9-10, 11-12, and on P7B 11-12 & 15-16.

This produces the memory timing shown in Fig 12.

U206 (AA491) decodes BUS-RAE/, BUS-CAE/, VIDEO-RAE/, & VIDEO-CAE/.

U206 (AA492), U186, U54 (AA502), & U55 (AA500, AA501, XX45, XX46) provide the RAS timing and bank selection using LLA1 & LLA2.

4.3. Memory Addressing (Sheet 12)

This sheet contains the memory addressing logic used on a System (ie Processor Block) Cycle (ie not a Video Cycle).

U165 latches the Upper 5 address bits, to give UPPER-MADR(0-4). This buffer is enabled when VIDEO-CYCLE is low.

U123 compares UPPER-MADR(0-4) with the system DRAM base address, programmed on P4, to decide if the on board DRAM is being addressed. If it is, U123 asserts CAS-EBL.

A link on P4 represents a '0' in the corresponding bit of the address, & no link represents a '1' (because of the pull-up RP1).

If 64K DRAMs are being used, pins 1-2 & 3-4 should be linked to allow all bits of UPPER-MADR(0-4) to be compared.

Pins 5-6, 7-8, 9-10, 11-12, 13-14 then allow the base address to be set on any 512KByte boundary in the 16MByte address range (however, as discussed earlier, other features of the MG-1 Memory Map resrict the DRAM to the lower 8MBytes of the address range - so Pins 13-14 of P4 should always be linked!).

Pin A5 of U123 is pulled high, thus if pins 15-16 of P4 are linked, the on board DRAM can never be accessed i.e. it is disabled.

If 256K DRAMs are being used, the RAM needs to be addressed in 2MByte blocks. This is done by omitting the links on 1-2, 3-4, 5-6 & 7-8.

In a 64K DRAM system, U247 & U246 used to enable the ROW & COLUMN addresses (respectively) onto U-MUX-MARD(0-7).

256K DRAM systems require 9-bit ROW & COLUMN addresses - the extra bit is decoded from UPPER-MADR0 & UPPER-MADDR1 by U166.

U-MUX-MADR(0-8) is sent to the Memory Expansion connector J11, and is used on board by U95 & U119 (via the damping resistors) to give the DRAM multiplexed addresses MUX-MADR(0-8).

During a Read-Cycle, U104 & U154 generate RBS(0-3)L & RBS(0-3)H from LLA1-2, BHBE, LLA0 & SYSTEM-DRAM/. These signals are used to enable the appropriate bytes of data from the memory system (which is read 8-bytes at a time) onto PB0-15.

Similarly, U53 & U163 generate the Write Enable signals WE-(0-3)L & WE-(0-3)H.

4.4. Low Byte Memory Banks (Sheet 15)

This contains the 32 chips that make up the low bytes of each 16-bit word in the array (labelled 0L, 1L, 2L & 3L).

MUX-MADR(0-8) & CAS/ is taken to each chip.

To write to the array, PB0-7 is buffered by U19 (& damped by U20) to give WD0-7, which is taken to the corresponding bit of the array.

WE-(0-3)L enable writes to the appropriate bytes.

RAS0-3/ enables memory cycles to be done to individual bytes.

Data is read out onto 0L(0-7), 1L(0-7), 2L(0-7) & 3L(0-7).

4.5. High Byte Memory Banks (Sheet 16)

As Sheet 15, except that it contains the high-bytes.

5. The I/O Processor Block

As mentioned, earlier the MG-1 uses a separate microprocessor to look after I/O operations such as keyboard, mouse & cursor. The microprocessor used is the Motorola 68121 which is specifically designed for use in this type of situation.

The 68121 is an 8-bit device with a 6801-type instruction set. It contains 128-bytes of Dual-Ported RAM with which it can communicate with the host-processor. It can be configured in one of two modes (called Mode 2 & Mode 3). The MG-1 uses Mode 2 which gives a 64KByte address range, with the 68121 internal registers & RAM mapped into the first 256-bytes of memory. See Fig. 10 for IOP Memory Map.

5.1. IOP, ROM, RAM & Support (Sheet 21)

Fig. 11 shows the timing & control signals for an IOP Bus Cycle.

U327 is configured as 4-bit shift register clocked at 8MHz with its inverted output fed back to its input - producing four phase-shifted 1MHz square waves. U327 is held clear until power is stable by POWER-OK, which ensures that the shift register begins clocking from a known state.

The outputs are gated using various bits of glue (U300 (AA342), U178 (AA128), U307 (AA336), U326 (AA334)) to give IOP-AS, IOP-RD/, IOP-WR/ & IOP-CE/.

- IOP-AS is the IOP Address Strobe. U289 latches the lower 8 address bits of AD0-7 using this signal.
- IOP-RD & IOP-WR/ are the masked Read & Write strobes. They are valid during the Data Time of each bus cycle, and are high during the Address Time.
- IOP-CE/ is used to enable address decoding once addresses have become stable.

U274 (AA579) buffers IOPE, raising its voltage. If the IOP is driven with a normal TTL output it will not work.

Because the IOP clock (E) has been delayed by U274 (AA579), it is not possible to use IOPE as the OE/ signal for the Data Bus Buffer, U283, therefore the 'QB' output from U327 is used.

The address decoding for the ROM (U285) & RAM (U284) is done by U285 (BB12), & U307 (AA335).

U276 (AA332) synchronises the RESET signal to IOPE and U274 (AA580) brings the voltage to an acceptable level.

U276 (AA689) & U300 (AA445 & AA446) ensure that, during RESET, pins 43 & 45 of the IOP are held low. This, together with pin 44 set high, sets the IOP into Mode 2.

At all other times, pin 43 is used as an interrupt input, & pin 45, as the Serial Clock input.

Note: The IOP has an on chip USART. This is used on the MG-1 to accept serial data from the keyboard (J1). KBRD-DATA & KBRD-CLK are buffered by U330 (AA330 & AA331).

5.2. CTC & Mouse Counters (Sheet 22)

The IOP CTC (U286) controls the Cursor position (Channels 1 & 2, both programmed in CTC Mode 1) & the Front Panel Buzzer (Channel 0, CTC Mode 3). Channel 0 is clocked at 1MHz by IOPE, & its output is taken to the speaker via U277 (AA756), R30, R31, C157 & C158. The sound output can be disabled by setting U328 (AA548) low by writing to X-CNT-CS with IOPD0 low.

U328 (AA549) allows the IOP to switch the screen on/off (DISP-SWITCH-ON).

5.2.1. The Mouse Movement Counters

The rest of the circuitry tracks the movement of the mouse, and consists of two identical counter sections - one for movements in the 'X' direction, the other for 'Y' movements.

Changes in the state of the XA & XB (or YA & YB) inputs are counted by the two cascaded up/down counters (U301 & U302 for X-movements, U308 & U309 for Y-movements).

These are clocked continuously by IOPE, but U312 (U305 for Y-movement) only enables the counters when a transition on the inputs has taken place. U287 latches the current status of the mouse inputs & their status at the previous IOPE rising edge.

This complicated arrangement allows the counters to be clocked on every transition of XA & XB (or YA & YB), giving greater resolution than otherwise would be the case.

U303 & U310 latch their respective counter values, & are enabled onto the bus when a read is performed from the appropriate location. This also clears the counters.

5.3. IOP Address Decode & Mouse Buttons (Sheet 23)

U306 performs the I/O address decoding for the IOP.

Writing to 'HOST-RESET' with Address Bit IOPA8 clear, issues an IO-RESET/, if IOPA8 is set, IO-RESET/ is negated (ie the effect of accessing this I/O area depends on which 'copy' of the I/O area the IOP is actually accessing).

IO-RESET is issued by the IOP as part is its initialisation routine. Its purpose is to cause another SYSTEM-RESET to be issued. This is necessary to overcome an MMU bug whereby, the MMU & CPU can sometimes become 'out-of-step' when coming out of reset after power-up. U276 (AA332) (Sheet 21) ensures that IOP is not re-reset when it issue an IO-RESET.

The secondary function of IO-RESET is to allow the IOP to reset the rest of the system when the user presses the 4 'corner' keys of the keyboard.

Writing to MOUSE-BUTTONS allows the IOP to select the CURSOR-OR-FN.

Reading from MOUSE-BUTTONS allows the IOP to monitor the state of the buttons on the mouse.

Accessing IOP-INTERRUPT causes an interrupt to be issued to the host processor - this is used to indicated that the IOP wants to be serviced by the host.

6. Power Distribution (Sheet 27)

The sheet contains the decoupling for the power rails, & various power on/off/fail indictation signals.

R38, C191 are the Power-On reset RC Network with a time constant of around 0.5 seconds. D13 allows C191 to discharge quickly when power is removed. U315 (AA659 & AA660) 'square' the signal up to give RESET-RC/.

SYSTEM-RESET/ is asserted if RSTSW/ (from the reset switch on the Power Distribution Board) or IO-RESET/ (from the IOP) or RST-RC/ is asserted.

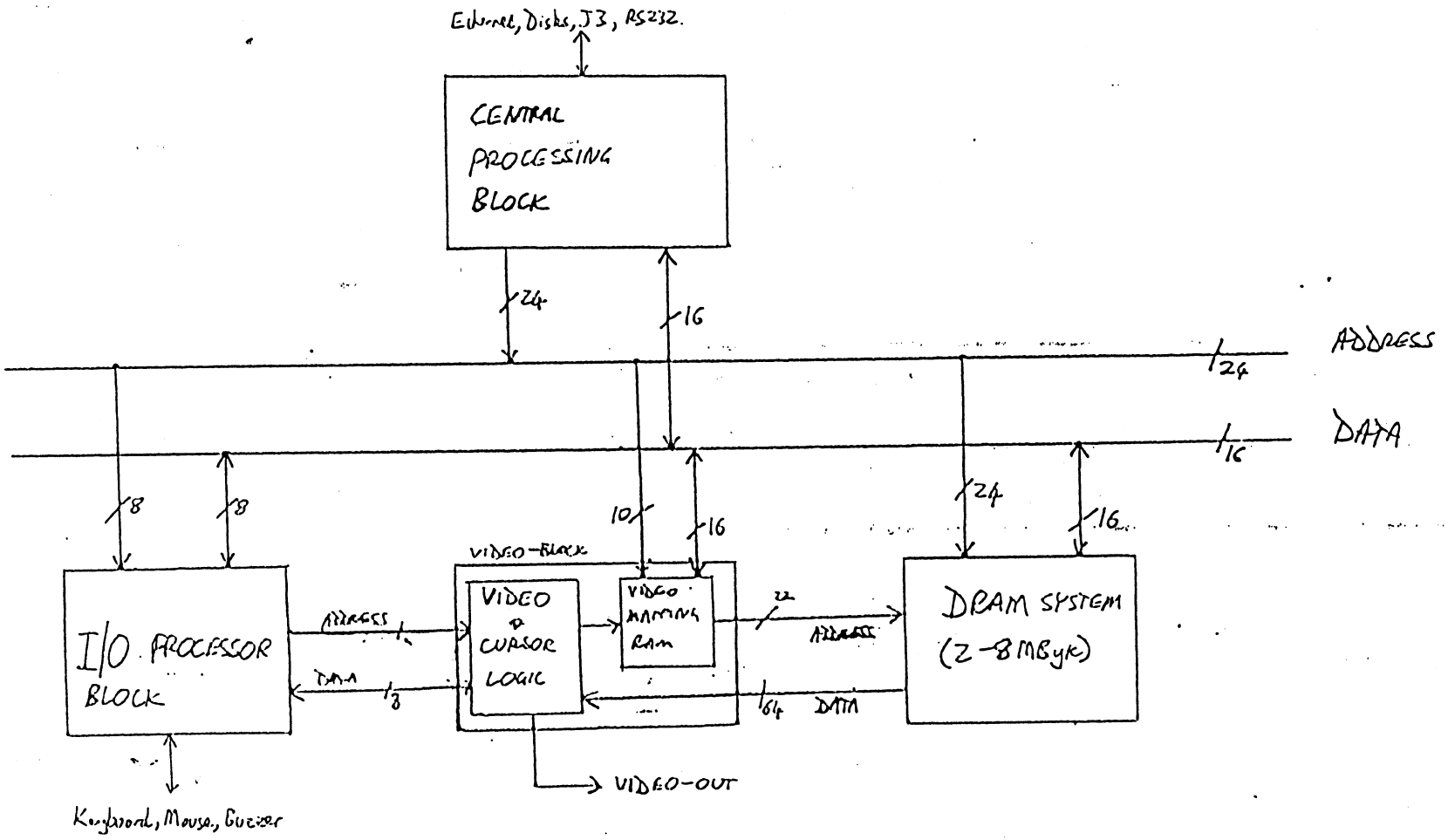
U321 is powered by VBACKUP, so POWER-OK & POWER-OK/ are valid even when the system is powered down.

POWERFAIL/ is taken to Sheet 1 to give the CPU the NMI high priority interrupt.

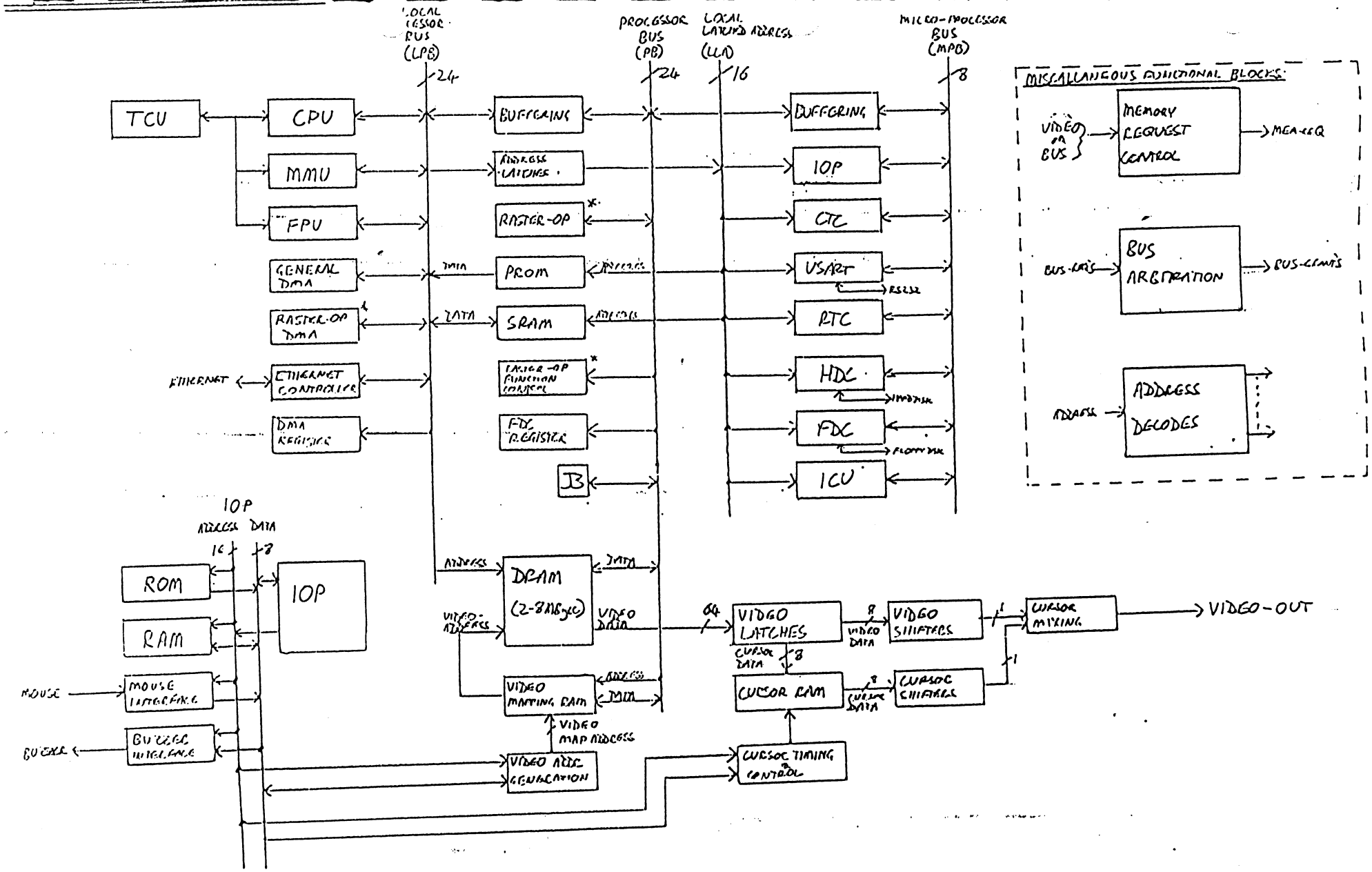
7. Spare Gates & Components (Sheet 28).

This sheet contains the list of unused gates & components not shown elsewhere in the cct diagrams.

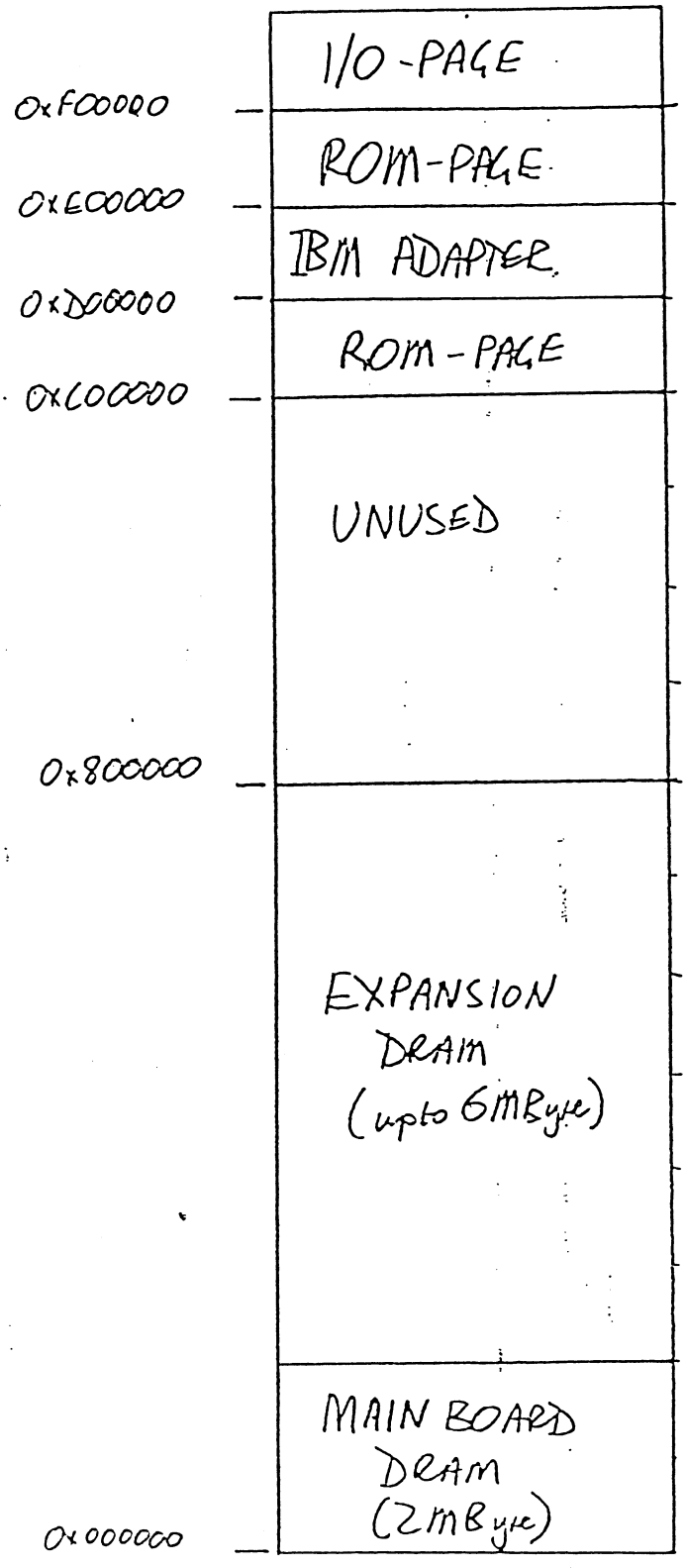
Fig1: MG-1 MAIN BOARD OVERVIEW



[redacted] BLOCK DIAGRAM

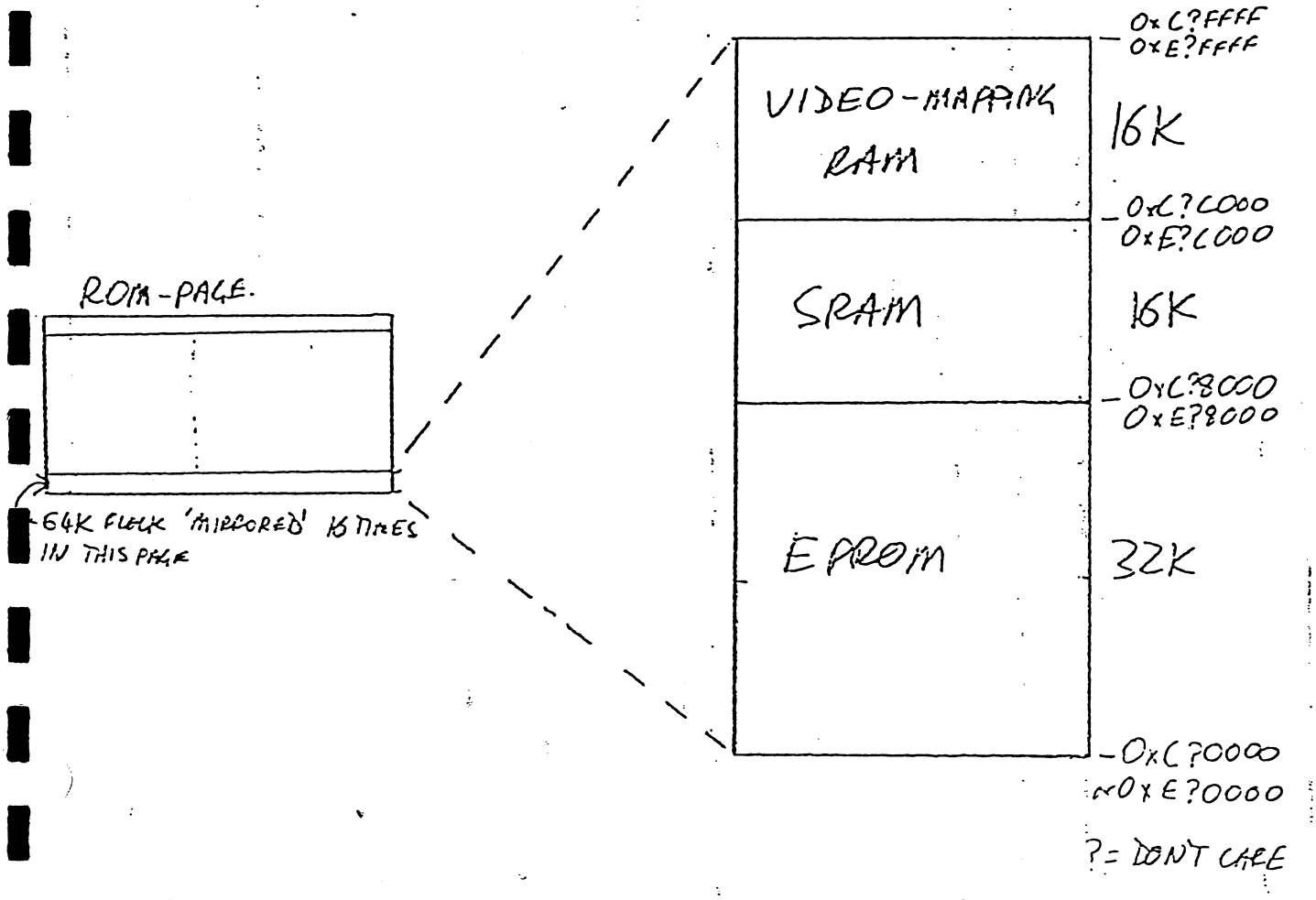


* - No Longer Used


I/O-PAGE
0xF00000
ROM-PAGE
0xEC0000
IBM ADAPTER
0xD00000
ROM-PAGE
0xC00000
UNUSED
0x800000
EXPANSION
DRAM
(upto 6MByte)
MAIN BOARD
DRAM
(2MByte)
0x000000

4. ROM-PAGE MEMORY MAP

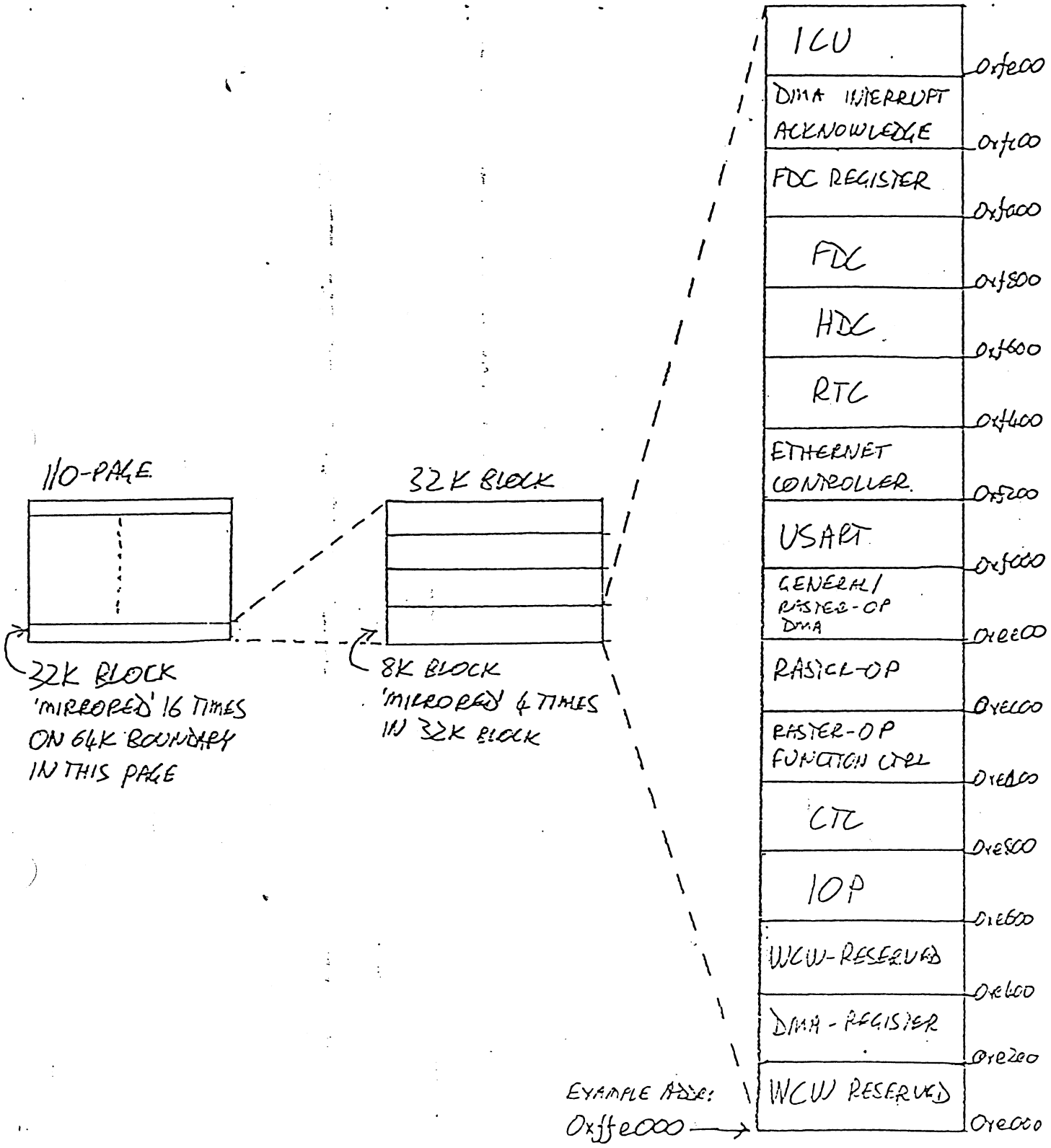
ROM 5/5/86

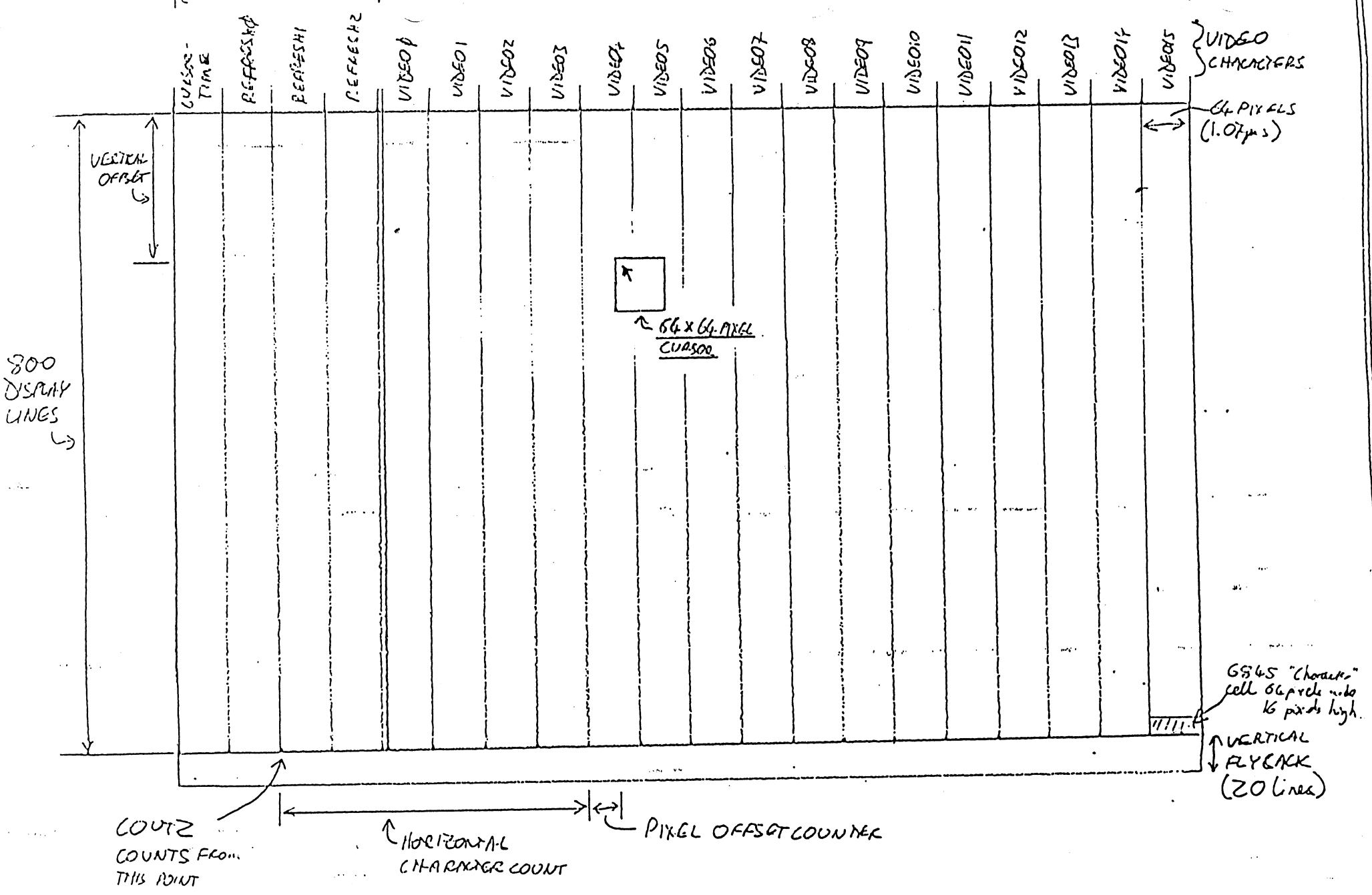


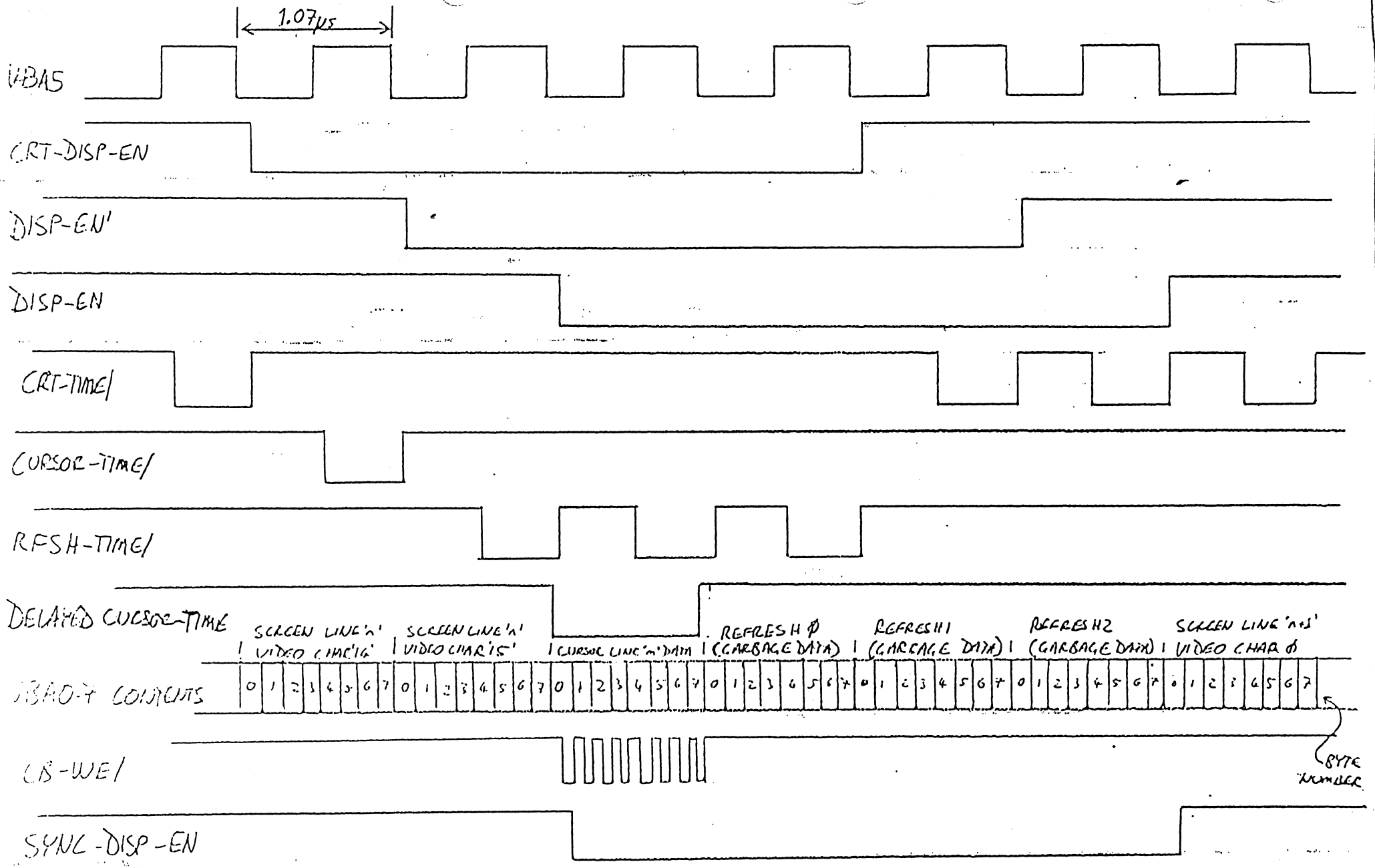
?= DON'T CARE

Fig 5: I/O-PAGE MEMORY MAP.

PDM 3/3/86




CURSOR TIME
REFRESH
REFRESH
REFRESH
VIDEO 0
VIDEO 1
VIDEO 2
VIDEO 3
VIDEO 4
VIDEO 5
VIDEO 6
VIDEO 7
VIDEO 8
VIDEO 9
VIDEO 10
VIDEO 11
VIDEO 12
VIDEO 13
VIDEO 14
VIDEO 15
VIDEO CHARACTERS
64 PIXELS (1.07 μs)
VERTICAL OFFSET
800 DISPLAY LINES
64 x 64 PIXEL CURSOR
6545 "character" cell 64 pixels wide 16 pixels high.
VERTICAL FLYBACK (20 lines)
COUNT COUNTS FROM THIS POINT
HORIZONTAL CHARACTER COUNT
PIXEL OFFSET COUNTER


1.07µs
VBAS
CRT-DISP-EN
DISP-EN'
DISP-EN
CRT-TIME/
CURSOR-TIME/
RFSH-TIME/
DELAYED CURSOR-TIME
SCREEN LINE 'n' VIDEO CHAR 'G'
SCREEN LINE 'n' VIDEO CHAR '5'
CURSOR LINE 'm' DATA
REFRESH 0 (GARBAGE DATA)
REFRESH 1 (GARBAGE DATA)
REFRESH 2 (GARBAGE DATA)
SCREEN LINE 'n+1' VIDEO CHAR 0
VBAD-7 CONDUITS
CS-WE/
BYTE NUMBER
SYNC-DISP-EN

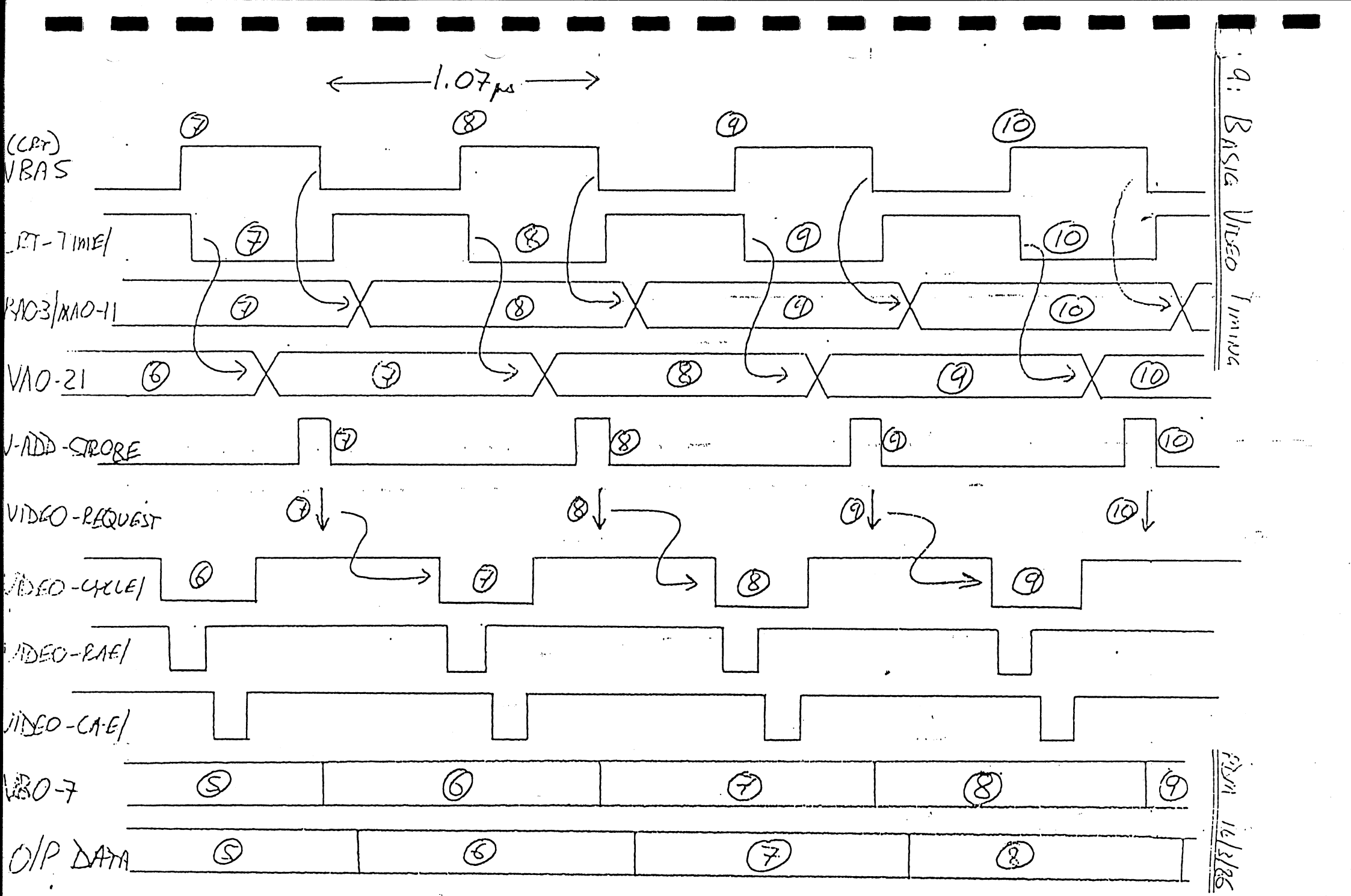
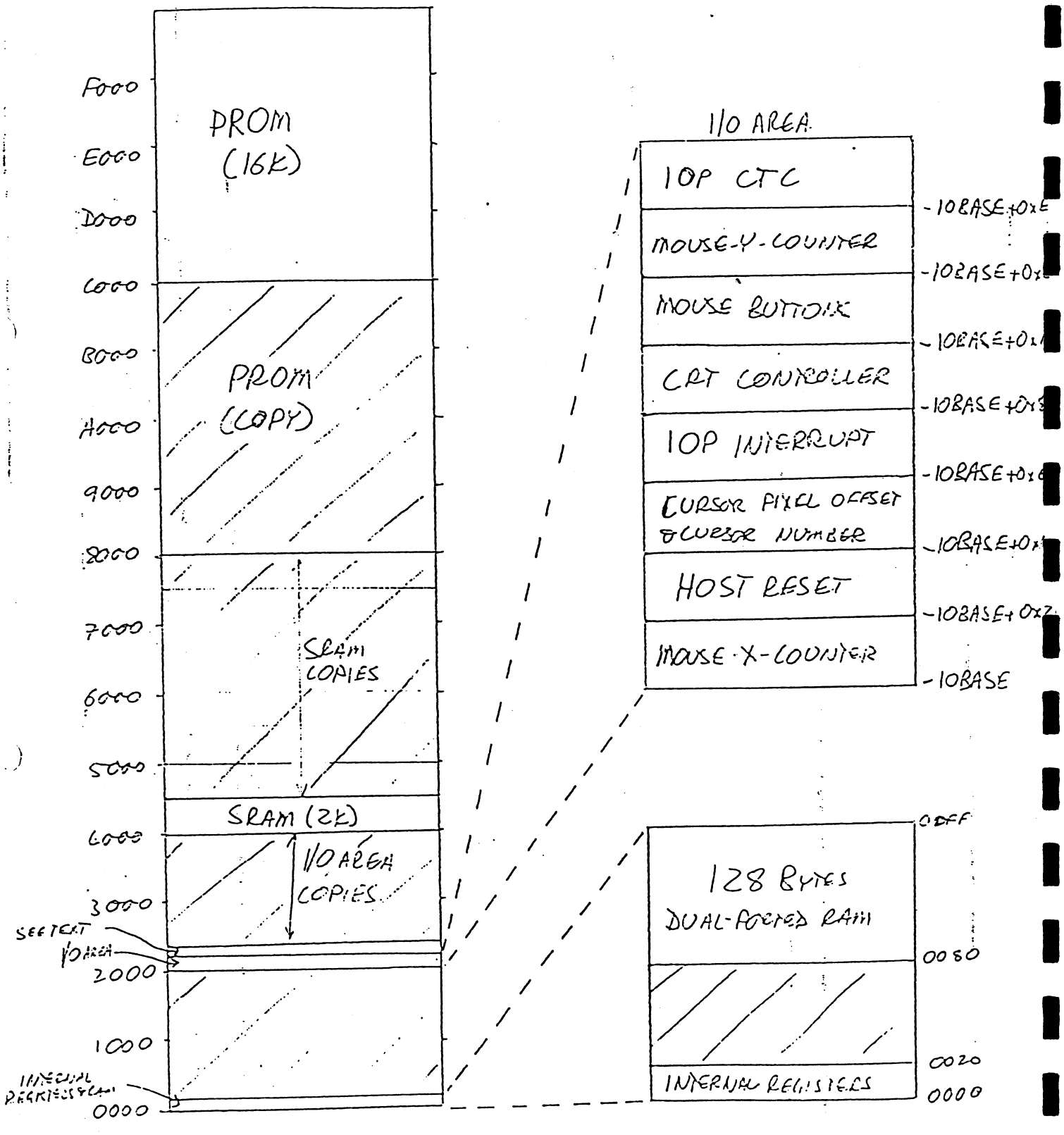


Fig 4: Basic Video Timing

FIGURE 11/5/26

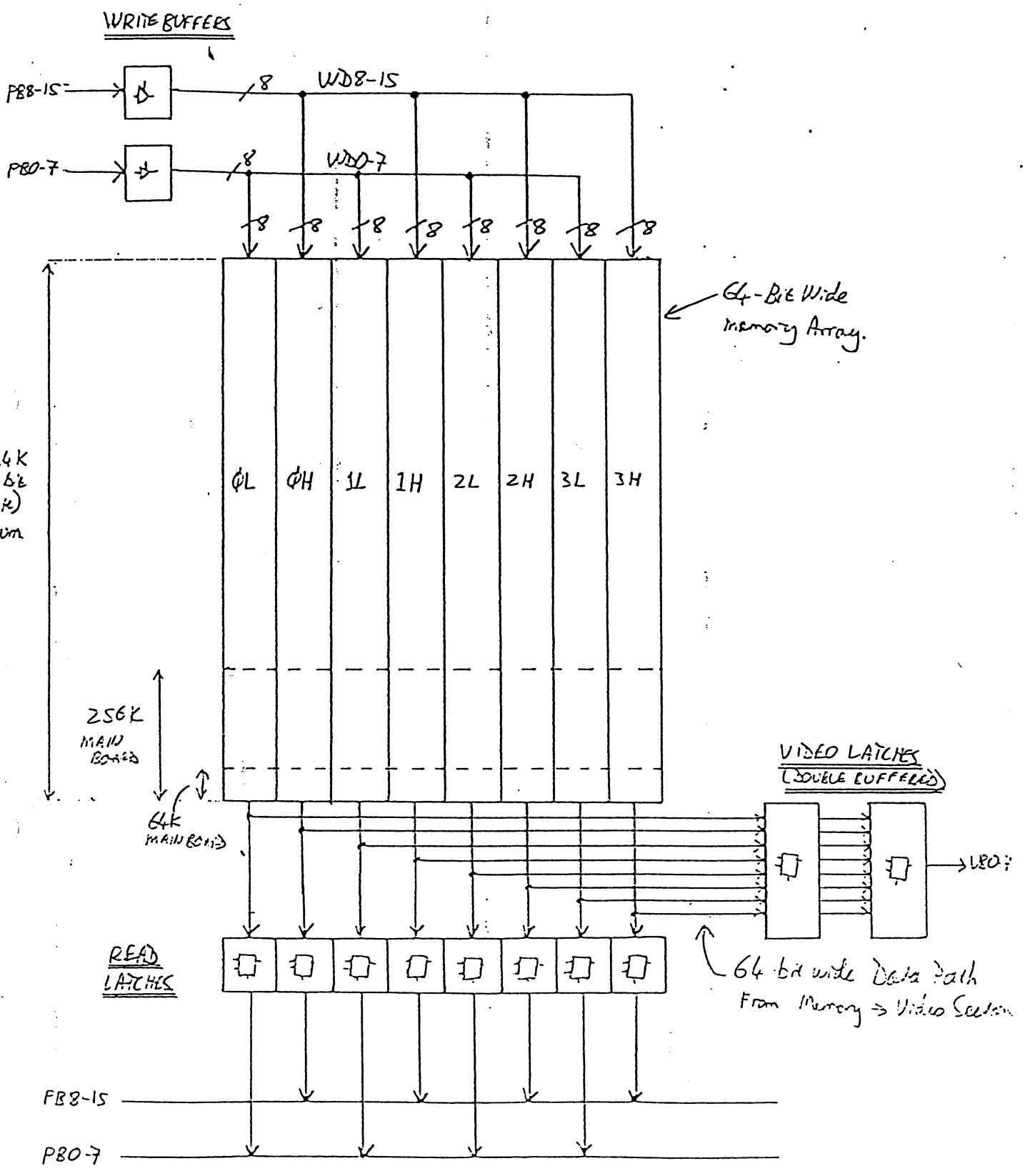
fig 10: THE IOP MEMORY MAP

PDM 18/3/86



8: THE MEMORY SYSTEM

PDM 11/3/86



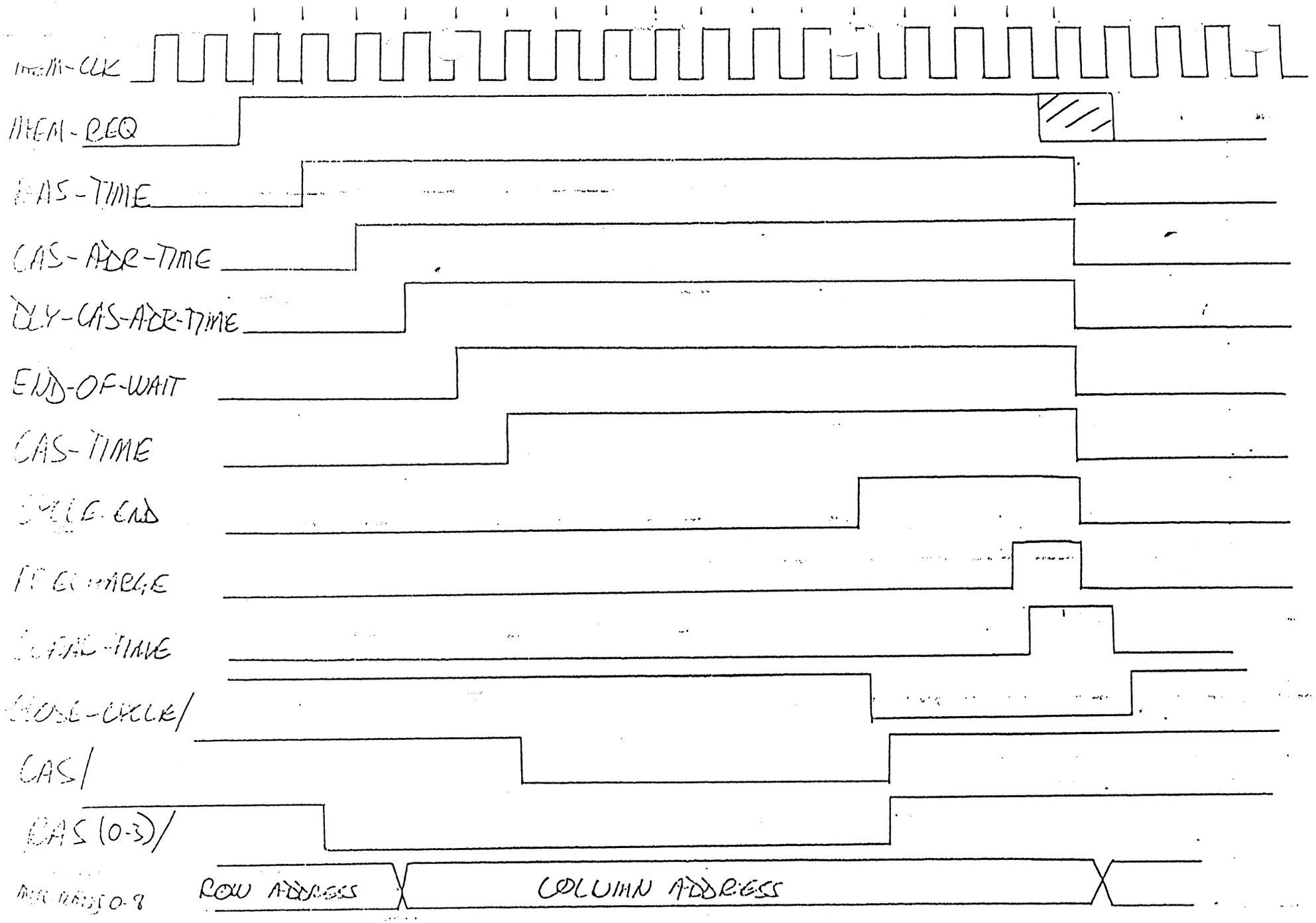


Fig. 12: Memory Timing

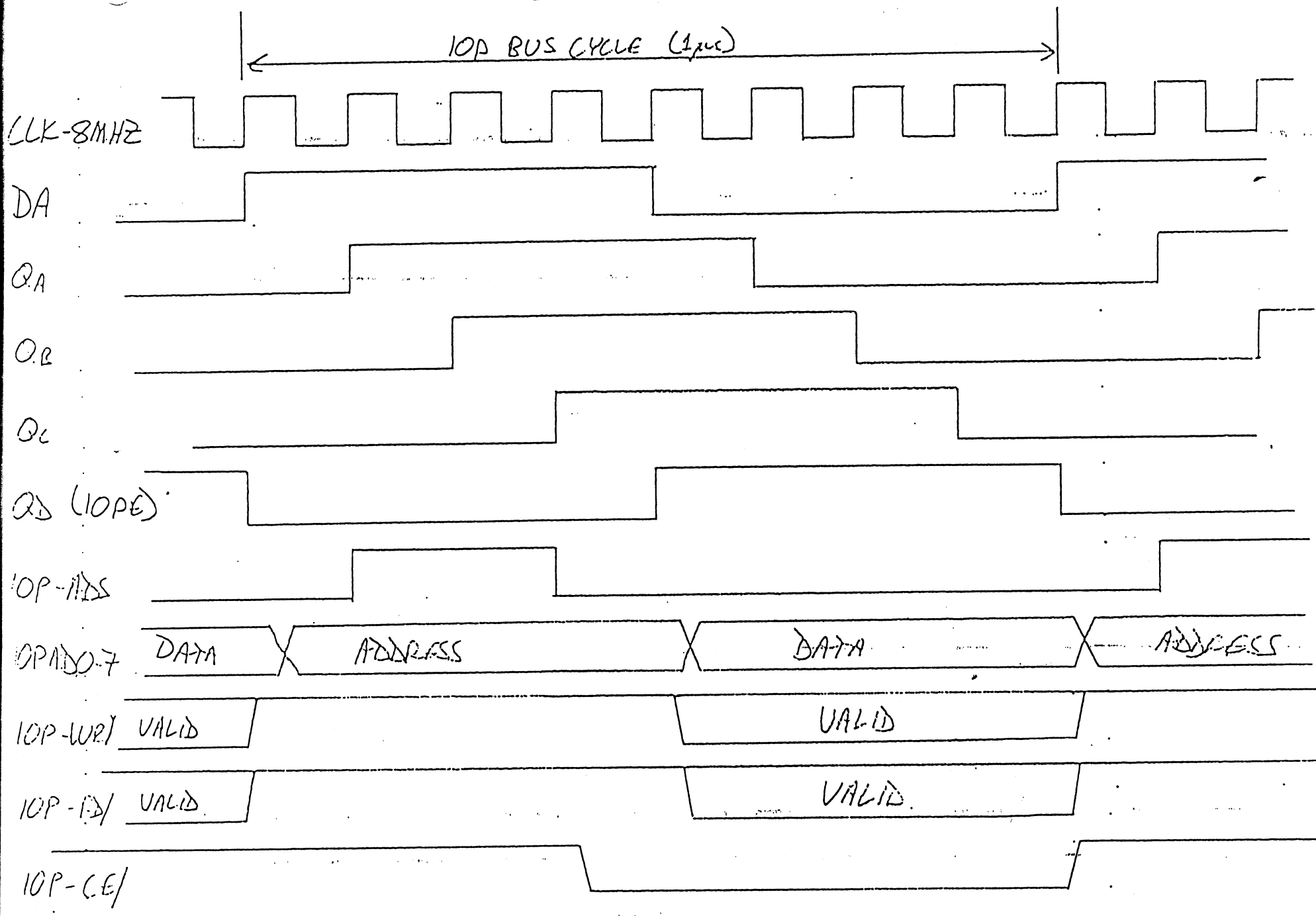


FIG 11: IOP TIMING & CONTROL SIGNALS

Support Note No 5

Jump Start Lead and Method

Equipment Required

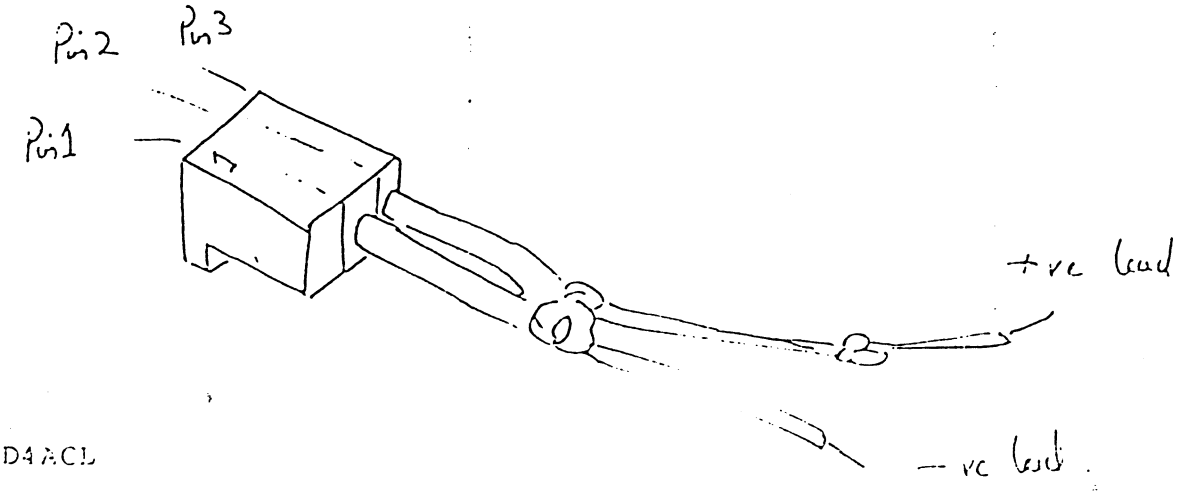
Item	WCW Part No	Description	Qty
1	W006 043 000	Correcta Female	2
2	W006 042 000	Shell Socket	1
3	----	Multi Strand Single Core Wire	12"
4	----	9v Battery	1

Overview

It has been found that under certain circumstances during transit the batteries on the Power Distribution Board become discharged, although this has no adverse effect upon the system, it makes normal 'powering on' of the system impossible. To power up the system it now requires a special connecting cable and battery pach.

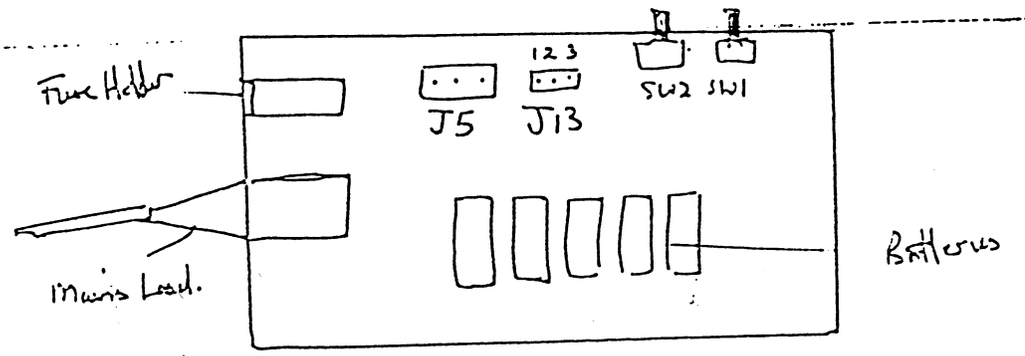
Jump Start Lead

the plug shell (Item 2) is marked with a "1" on the opposite side from the horns, the "1" indicates the location of Pin 1 which is not used. Pin 2 is the ve connection and the cable from this connector should be connected to the ve terminal of a 9v Battery. Pin 3 is the +ve connector and a cable should be taken to the +ve termainal of a 9v Battery. (It would be good practice to indicate this lead by inserting an additional in the +ve lead).

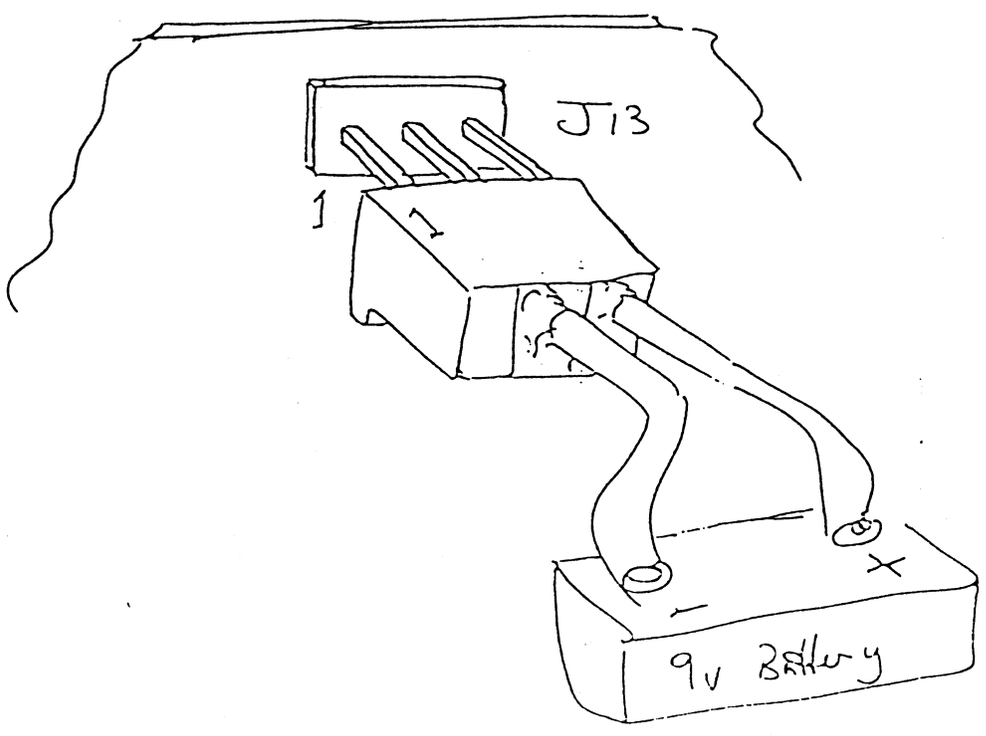


Connection to Power Distribution PCB

Examin Power Distribution PCB and locate Plug Connector J13, which is the plug to which the Jump Start Connector Lead is to be connected.



Connect Jump Start Lead to J13. (Pin 1 on plug to Pin 1 on the connector of the Jump Start Lead). After system boots, carefully remove lead and then leave system running for a period of 15 minutes so that the startup batteries have recovered a sufficient charge before Powering Off the system.



SUPPORT NOTES NO. 7

CRT Adjustments to the Monitor Unit of the MG-1

Overview

It will occasionally become necessary to make field adjustments to the present controls of the CRT Monitor on the MG-1 workstation.

Caution

i) Flashover Protection

The primary function of the crt spark protection circuitry is to protect the monitor circuits from damage in the event of an internal flashover in the crt. When a flashover occurs, the crt final anode capacity which is approximately 1000pf charged up to 16-18kv is abruptly discharged, generating currents of several hundred amperes with durations up to 100nS. The spark protection is instrumental in routing these currents into well defined low impedance paths and preventing the build up of voltage spikes which can break down solid state devices.

Therefore ensure that all connectors are currently connected before powering up the crt after any adjustments.

(ii) Discharge Procdure

Before attempting to remove a crt from its mounting, it will be necessary to discharge the PDA (Extra High Voltage) connector which is covered by a protective insulating cap.

Remove all power supplies from the crt unit and wait 5 minutes for internal discharge. Then with two insulated handled screwdrivers, locate one on a good earth point on the chassis, place the other screwdrivers point underneath the protective cap. Without touching any other surface, component or yourself, bring the two metal shafts of the screwdriver, so discharging the crt.

(iii) Implosion Precautions

Although the Ccrt is fitted with Implosion bands, there is always the danger that when a crt is being moven that an accident can occur whereby the crt's envelope will rupture, with a subsequent danger to the person handling the crt receiving injury from fragments of glass.

All persons handling a crt should be wearing the following items:

a) Gauntlets to protect the hands
b) A Class 1 British Standard BS2092 (impact resistant) face visor with headband, to protect face and eyes.
c) Canvas apron to protect those other precious parts.

(iv) Xray Emission

Less than 0.5 mRads per hour
EHT voltage nominal 16.5Kv
(limitary EHT value on this CRT is 23Kv.

(v) Adjustments Precautions

The crt unit of the MG-1 contains voltages which are dangerous therefore compliance with the Health and Safety at Work Act are necessary.

a) A competant person should be present at all times while making the adjustments, this person should be familiar with how to switch the equipment OFF in an emergency.

b) All other safety precautions should be observed.

SPECIFICATION OF THE CRT

CRT Diagonal	17 Inches
CRT Phosphor	White (P4)
Dot Clock	60 MHz
Display Density	1024 pixels (Horiz)
	800 pixels (Vert)
Line Frequency	46.877 KHz
Frame Frequency	56 Hz
Non-Interlaced	
Line Sync Pulse Width (& Polarity)	1.066 uS (+ ve)
Frame Syne Pulse Width (& Polarity)	341.32 uS (+ ve)
Active Video Line Time	17.066 uS
Active Video Frame Time	17.066 mS

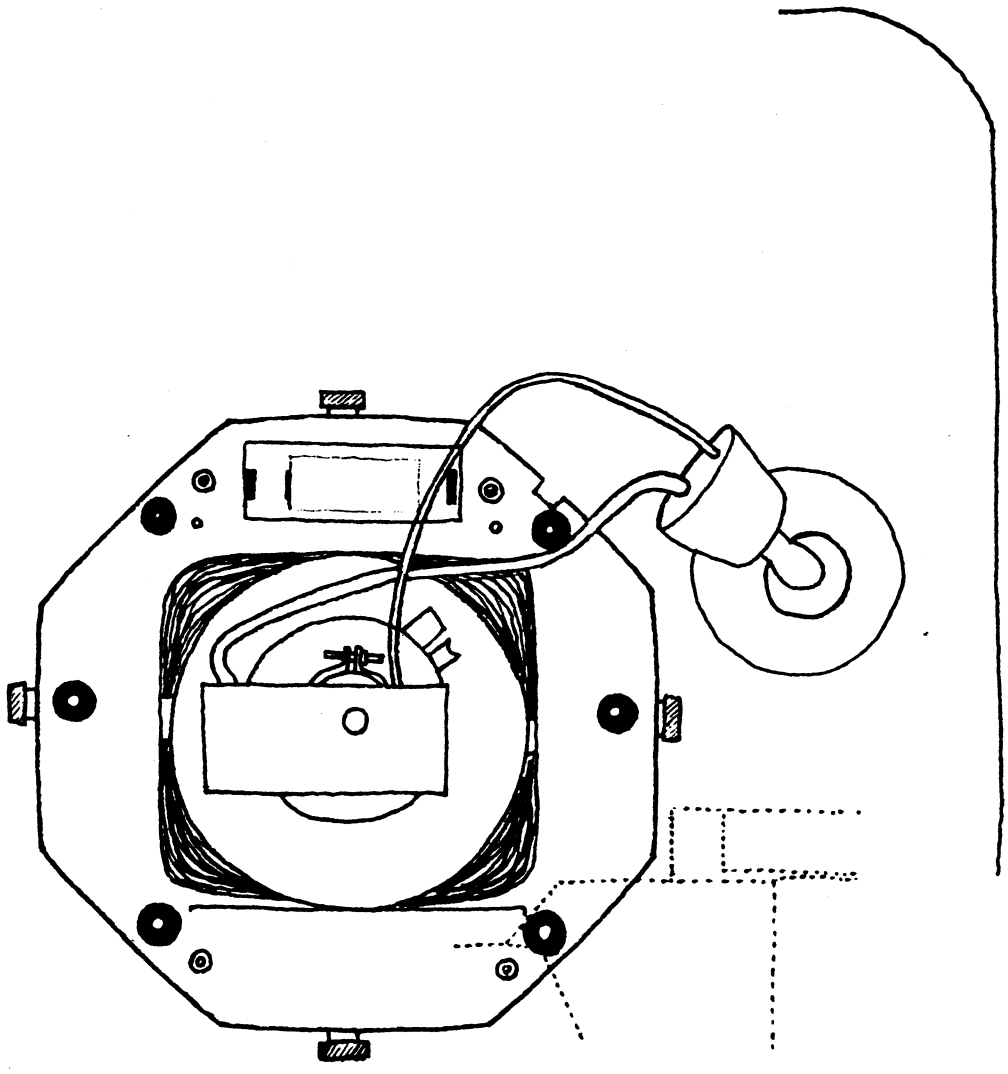
RECOMMENDED SET-UP PROCEDURE

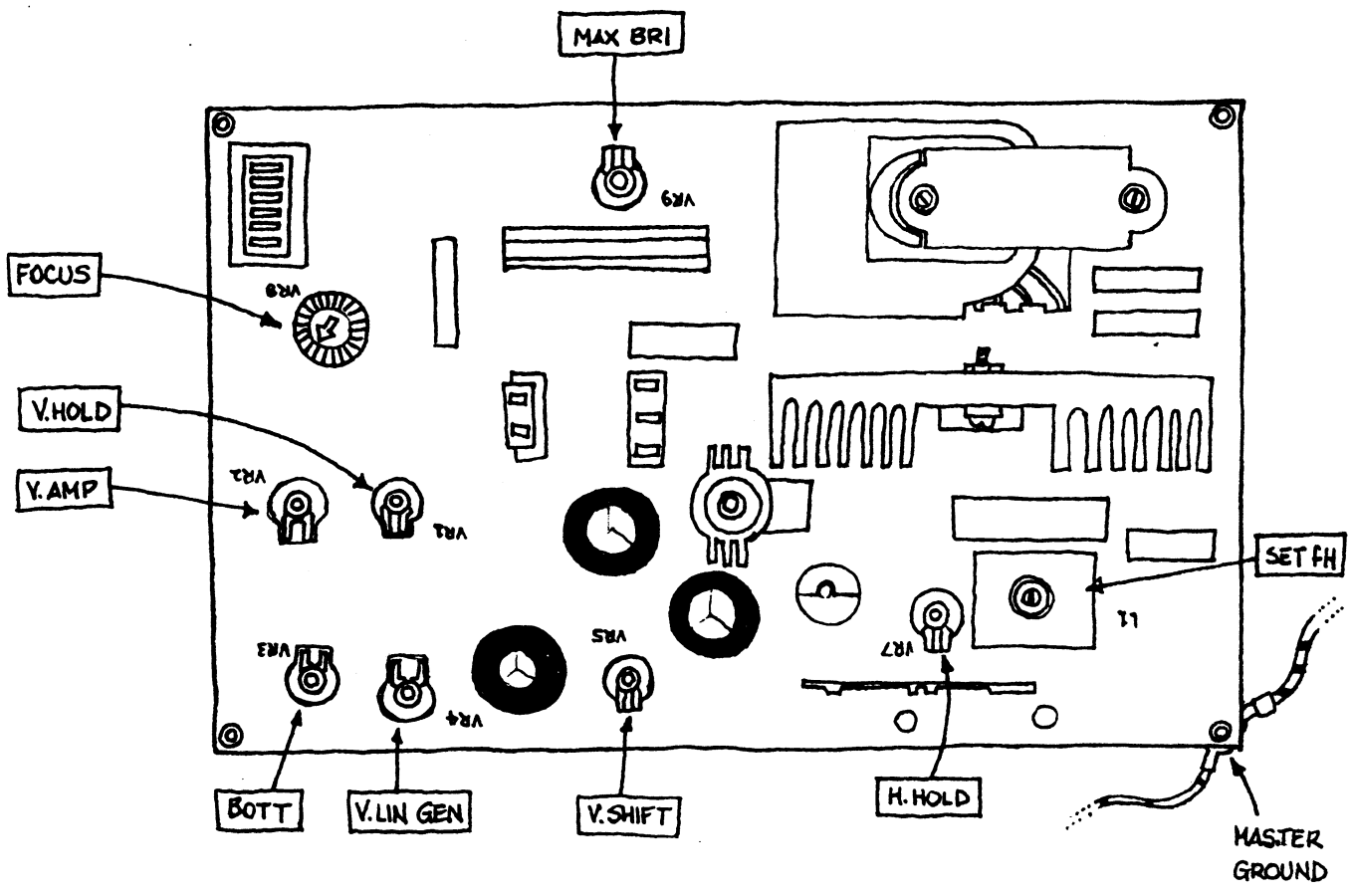
It is assumed that the assembly to be set up, has previously been set up correctly during manufacture and that all the components are present and in the correct positions with correct values, and where appropriate, polarities, and that there are no defective parts.

EQUIPMENT REQUIRED

a) Test generator with at least crosshatch, and preferably circle and full page text capability.
b) Copper bladed trimming tool (A).
c) 0.1" square linearity adjustment tool. (B)
d) Various screwdrivers.
e) Supply of geometry adjustment magnets (by manufacture only).

Access to the crt of the Monitor is by removing the two covers, which are held in place by four Phillips Head belts shown in the diagram below.




MAX BRI
VR9
FOCUS
VR8
V.HOLD
V.AMP
VR2
VR1
SET FH
L1
VR7
VR5
VR3
VR4
BOTT
V.LIN GEN
V.SHIFT
H.HOLD
MASTER
GROUND

VERTICAL AMPLITUDE (HEIGHT)

Adjust VR2 (V.AMP.) to give a display of approximately the desired height.

HORIZONTAL LINEARITY *

A crosshatch and/or circle pattern should be displayed for this adjustment.

With tool B rotate the magnet in L2 (H.LIN) to give a display of maximum width, then continue to rotate until the left hand side of the display is at optimum linearity, ie. information at the left hand side of the display is as near the same size as that at the centre and right hand side as is possible within the limits of the control.

FOCUS

The test pattern should be changed to a full page of text. Adjust VR8 (FOCUS) to give optimum focus over the entire display area.

VERTICAL LINEARITY

The test pattern should revert to a crosshatch.

Adjust VR4 (V.LIN GEN) to equalise the height of blocks at the top of the display with those at the centre.

Adjust VR3 (V.LIN BOTT) to equalise the height of blocks at the bottom of the display with those at the centre.

At this point reset height if necessary. Adjustments to the vertical amplitude (Height) and this the vertical limearity are interdependent and may require to be repeated until the desired performance is achieved.

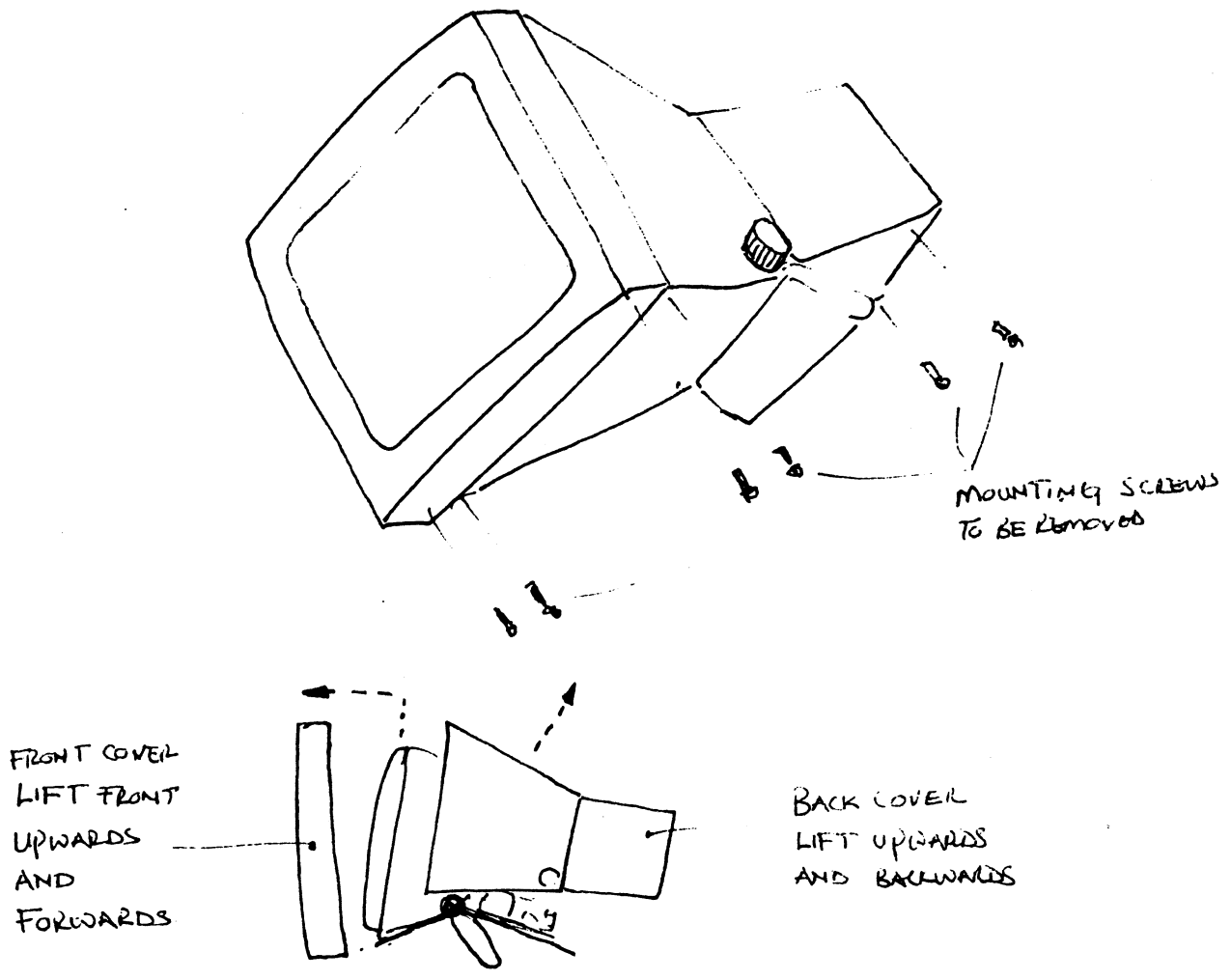
CENTRALISING THE DISPLAY

See caution section before attempting this adjustment

If necessary, readjust the concentric ring magnets on the scan coil to centralise the raster within the face of the crt. In order to achieve the best focus, it is important to use these magnets to centralise the raster only and not the information. When finished, seal to prevent accidental movement.

VERTICAL CENTRALISATION OF THE DISPLAYED INFORMATION

Rotate VR5 (V.SHIFT) to centralise the information within the face of the crt.



VERTICAL HOLD *

Adjust VR1 (V.HOLD) to find the points at which the field lock is lost in either direction and set the slider midway between these points.

HORIZONTAL ORTHOGONALITY *

See Caution section before attempting this adjustment.

Slacken the clamp screw on the scanning coil and rotate the coil until the centre line of the display is horizontal. Make sure that the scan coil is pushed hard up the neck of the crt towards the face and tighted the clamp screw.

RASTER POSITION

Rotate the concentric ring magnets at the rear of the scan coil to position the raster centrally within the face of the crt.

HORIZONTAL CENTRALISATION OF THE DISPLAYED INFORMATION

Correct operating conditions for the horizontal timebase have to be set before setting the position of the information.

The horizontal sync input at PL1/H has to be shorted to OV to remove it from the hybrid H3. The core of L1 is then adjusted to give a 'floating' picture, ie almost in lock even without sync. The short is then released and the picture will jump into lock. The core of L1 should be sealed to prevent disturbance in transportation and so on.

Rotation of VC1 will allow the displayed information to be centralised within the raster.

SETTING MAXIMUM BRIGHTNESS * (MB1700 ISS B ONWARDS)

VR9 (MAX BR1) should be rotated fully counterclockwise and, either VR6 rotated fully clockwise or the user brightness control set for maximum. VR9 is then adjusted to the point where the background raster is just visible.

HF ADJ (CRT BASEBOARD)

A full page of text should be displayed on the crt with the normally used polarity ie black on white or white on black. In the black on white mode the brightness must be turned down to a low level and the core of the coil screwed in to the point where a white overshoot to the right of the vertical bits of information becomes apparent. How much overshoot is acceptable is a matter of individual choice but going too far will cause severe 'ringing'.

PICTURE GEOMETRY ADJUSTMENT

Fit and adjust magnets as necessary around the periphery of the scan coil to give the best shape of displayed picture. Seal when finished to prevent accidental movement.

KENT MODULAR ELECTRONICS LIMITED

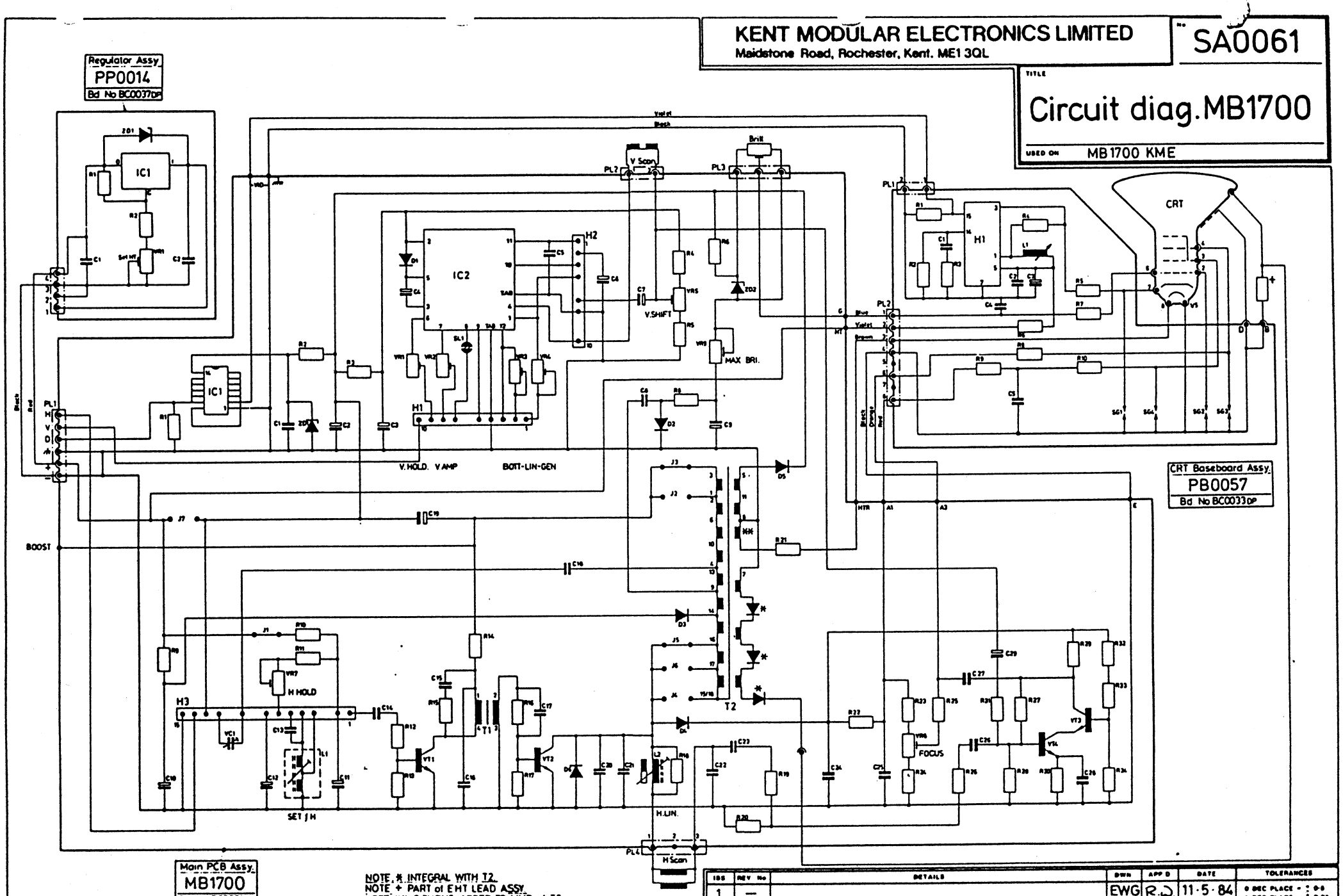
Maidstone Road, Rochester, Kent. ME1 3QL

SA0061

TITLE

Circuit diag.MB1700

USED ON MB1700 KME



NOTE * INTEGRAL WITH T2.
NOTE + PART of EHT LEAD ASSY.
NOTE ** 2 TURNS ADDED TO LIMB of T2.

ISS	REV No	DETAILS	DWN	APP'D	DATE
1	—		EWG	R.J.	11·5·84

TOLERANCES

0 DEC PLACE	± 0·5
1 DEC PLACE	± 0·25
2 DEC PLACE	± 0·1
3 DEC PLACE	± 0·05
ANGULAR DIMS	± 30

SCALE NTS

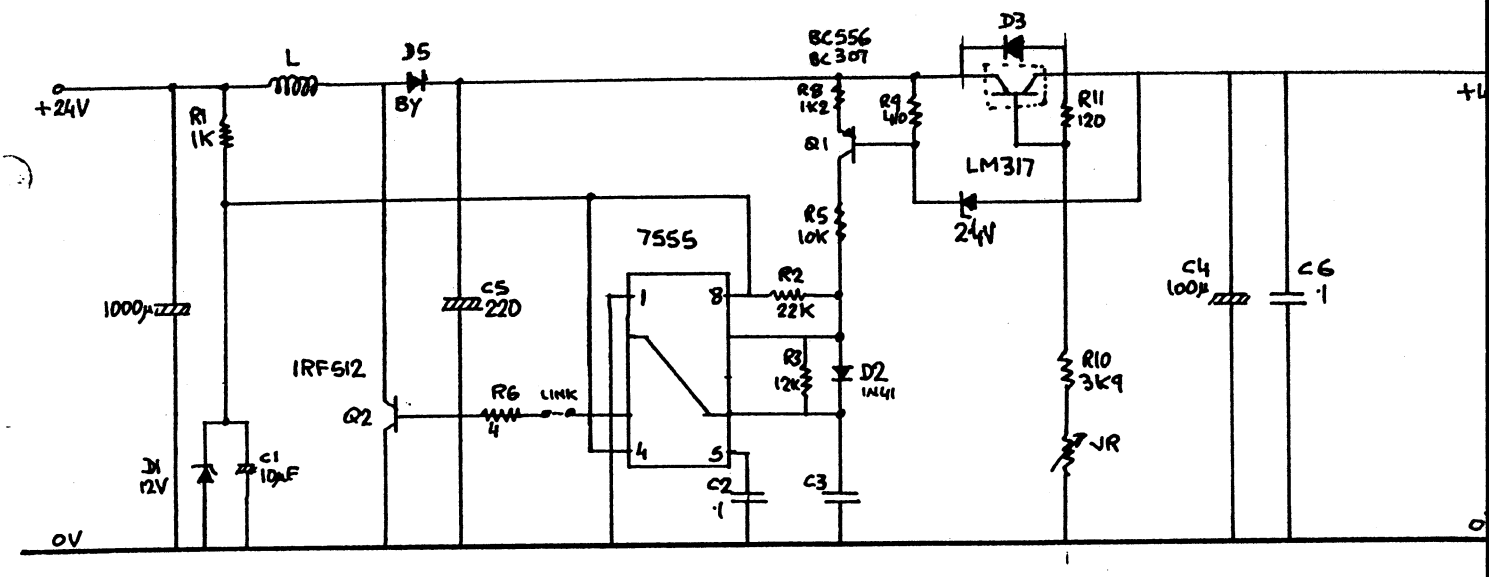
DIMENSIONS IN MILLIMETRES

DRAWN TO BS 308

DO NOT SCALE

CIRCULATION CODE

ABCHJNP



MG-1 Monitor Power Supply

SUPPORT NOTE NUMBER 8

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Therefore ensure that all connectors are currently connected before powering up the crt after any adjustments.

(ii) Discharge Procdure

Before attempting to remove a crt from its mounting, it will be necessary to discharge the PDA (Extra High Voltage) connector which is covered by a protective insulating cap.

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d) Various screwdrivers.
e) Supply of geometry adjustment magnets (by manufacture only).

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HORIZONTAL CENTRALISATION OF THE DISPLAYED INFORMATION

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Rotation of VC1 will allow the displayed information to be centralised within the raster.

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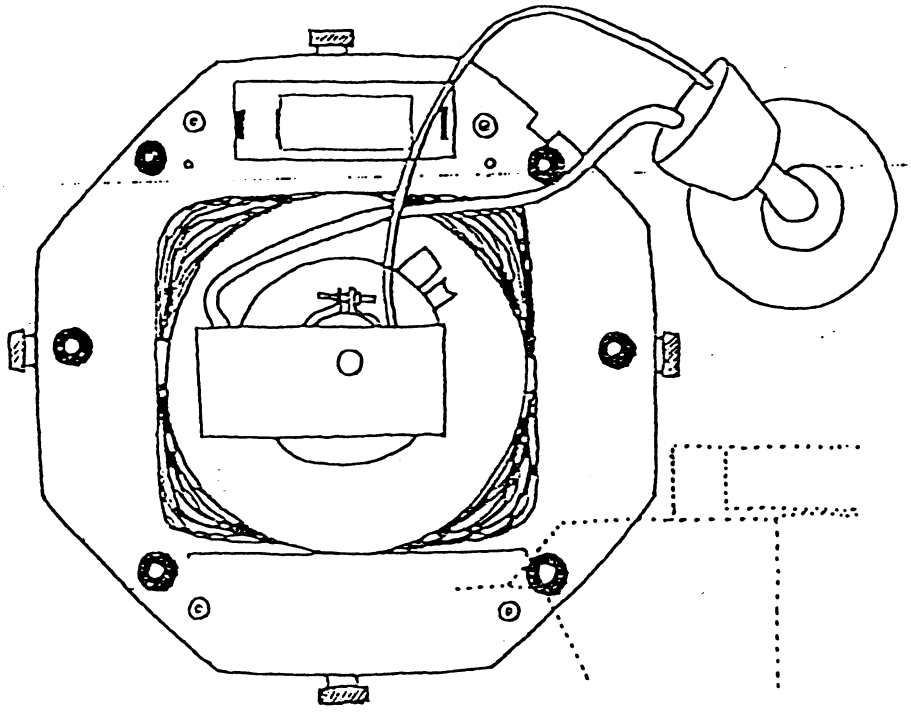
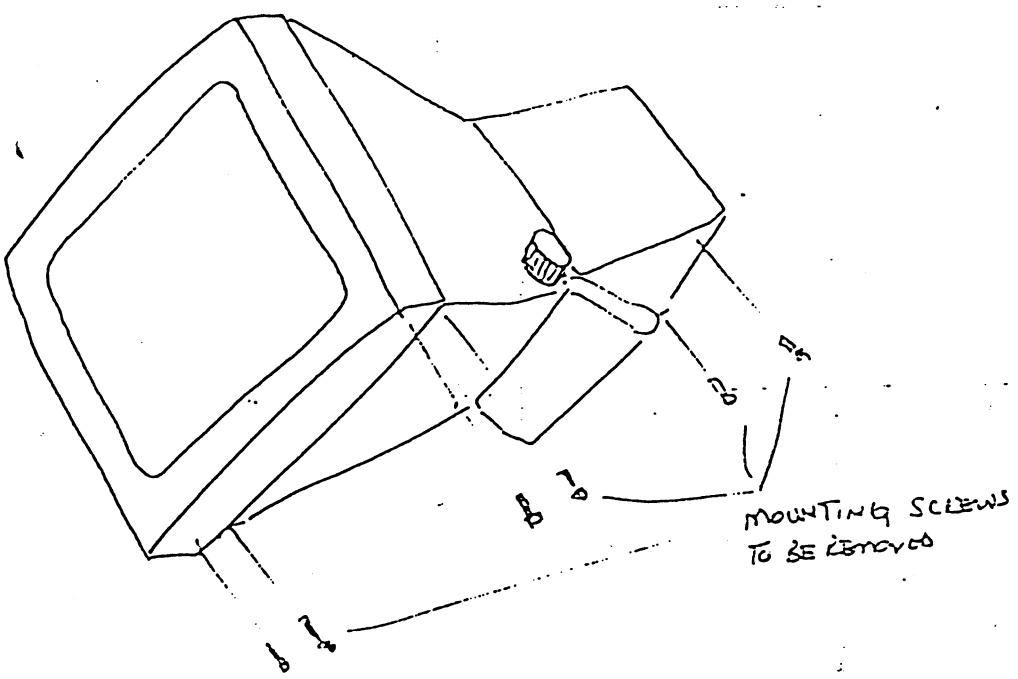
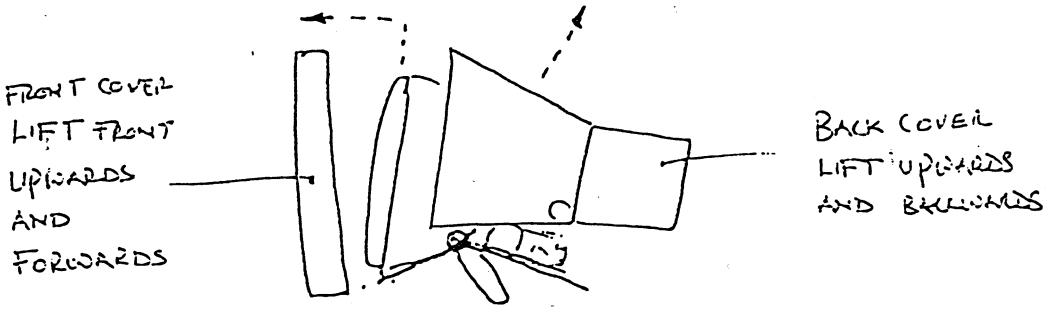
PICTURE GEOMETRY ADJUSTMENT

Fit and adjust magnets as necessary around the periphery of the scan coil to give the best shape of displayed picture. Seal when finished to prevent accidental movement.







VERTICAL HOLD *

Adjust VR1 (V.HOLD) to find the points at which the field lock is lost in either direction and set the slider midway between these points.

HORIZONTAL ORTHOGONALITY *

See Caution section before attempting this adjustment.

Slacken the clamp screw on the scanning coil and rotate the coil until the centre line of the display is horizontal. Make sure that the scan coil is pushed hard up the neck of the crt towards the face and tighted the clamp screw.

RASTER POSITION

Rotate the concentric ring magnets at the rear of the scan coil to position the raster centrally within the face of the crt.

VERTICAL AMPLITUDE (HEIGHT)

Adjust VR2 (V.AMP.) to give a display of approximately the desired height.

HORIZONTAL LINEARITY *

A crosshatch and/or circle pattern should be displayed for this adjustment.

With tool B rotate the magnet in L2 (H.LIN) to give a display of maximum width, then continue to rotate until the left hand side of the display is at optimum linearity, ie. information at the left hand side of the display is as near the same size as that at the centre and right hand side as is possible within the limits of the control.

FOCUS

The test pattern should be changed to a full page of text. Adjust VR8 (FOCUS) to give optimum focus over the entire display area.

VERTICAL LINEARITY

The test pattern should revert to a crosshatch.

Adjust VR4 (V.LIN GEN) to equalise the height of blocks at the top of the display with those at the centre.

Adjust VR3 (V.LIN BOTT) to equalise the height of blocks at the bottom of the display with those at the centre.

At this point reset height if necessary. Adjustments to the vertical amplitude (Height) and this the vertical limearity are interdependent and may require to be repeated until the desired performance is achieved.

CENTRALISING THE DISPLAY

See caution section before attempting this adjustment

If necessary, readjust the concentric ring magnets on the scan coil to centralise the raster within the face of the crt. In order to achieve the best focus, it is important to use these magnets to centralise the raster only and not the information. When finished, seal to prevent accidental movement.

VERTICAL CENTRALISATION OF THE DISPLAYED INFORMATION

Rotate VR5 (V.SHIFT) to centralise the information within the face of the crt.

SUPPORT NOTES NO. 9

Brief Resume of System ROM Error Codes and Their Interpretation

The error code numbering corresponds to the order in which tests are performed by the System ROM. Error codes are displayed by flashing the floppy LED - the 'on time' of the LED determines the digit value: 0 - short time, 1 - long time. All error codes are 4 bits in length.

Error Code	Error Type	Interpretation
0	ROM decode	The system ROM failed to detect its 'alias' in high memory (EF000) prior to switching DRAM on.
1	SRAM fail	Erroneous write/read operation on static RAM.
2	IOP fail	IOP has been unable to write to its dual-port RAM.
3	VMAP fail	Erroneous write/read operation on video mapping RAM.
4	ICU fail	ICU either not found or not responding to programming.
5	USART fail	USART either not found or not responding to programming.
6	Trap/NMI	Processor trap or NMI occurred prior to DRAM test.
7	Unused	-
8,9,A,B	Single-bit DRAM fail	Single bit error found. Bits 0-1 of error code indicate bank (0-3) containing error. A second code, displayed on keypress, will indicate the bank-bit (0-F).
C	Multi-bit DRAM fail	Multi bit error found. A second code, displayed on keypress, will indicate which bank contained the error (bits 1-2), whether more than one byte was involved (bit 3 set) and if bit 3 clear then which bank byte (bit 0).

Error Code	Error Type	Interpretation
D	DRAM address fail	Error discovered while writing/ reading locations with their own addresses. A second eror code is returned on keypress and is interpreted as for error C.
E	DRAM refresh fail	Contents of DRAM dropping out after time. Second error returned as for error E.
F	Unused	-

LINK OPTIONS

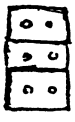
SUPPORT NOTE 12

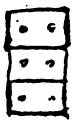
IBM CARD LINKS FOR LASER

P10 - 9, 10	11, 12 out	(default 11, 12 out)
P11 - 9, 10	out	(all in default)

LASER COMMAND MODULE LINKS

P1 

P2 

P3 

P4	9, 10	in
P5	4, 4	in
P6	3, 4	in

SCANNER CARD

Memory Address	XX00 H	(default 220 H)
Links	X2 X4 X6 X8 X10 X12	(all even jumpers on)

SUPPORT NOTES NO. 13

IBM Adaptor/Driver Preliminary Notes

1. Disclaimer

This document is provided in advance of formal documentation. WCW does not guarantee that it is full or correct, and reserves the right to make changes in the specification of the components described without notice.

2. Introduction

The MG-1 bus adapter is a motherboard accepting up to three IBM-PC compatible IO expansion cards. This document is a programmer's guide to the use of the bus adapter with proprietary or third-party expansion cards.

The PC bus used by the IBM PC and compatible micros is a de facto rather than a formal standard, although the number of different manufacturers making boards to the standard is testament to its effectiveness. This document and its accompanying diagrams should give sufficient information about the bus for simple interfaces. There are no specifications for timing; where common sense runs out the designer is best advised to consult the specifications of the 8088 microprocessor and the 8037 DMA controller on which the timings ultimately depend.

The bus strongly reflects the characteristics of the 8088 microprocessor, and great care has been taken to emulate these characteristics in the MG-1 bus adapter. The bus has the following signals:

[1] A 20-bit address bus and an 8-bit data bus.

[2] Addressable memory extends from 0 to hexadecimal DFFFF; there is also a 64kbyte IO space from 0 to hex FFFF.

[3] There are six interrupt levels (IRQ2-7), and one (IO_CH_CK) which in the IBM PC is connected to the microprocessor's non-maskable interrupt input.

[4] Request and acknowlegde signals are provided for three DMA channels (DRQ/DACK); the characteristics of the channels are determined by the 8037 DMA controller. In most IBM PCs three out of the four 8037 channels are used for system devices.

3. MG-1 Memory/Device addresses

The MG-1 uses memory-mapped IO; all of the locations on the IBM adapter are addressable by the MG-1 at the following locations:

IBM bus locations	MG-1 addresses
(memory) 0 - DFFFF	D00000 - DDFFFF
(i/o) 0 - FFFF	DE0000 - DEFFFF (normal access) DF0000 - DFFFFF (DMA access)

Width — Although PC bus memory can only be 8 bits wide, the MG-1 bus adapter will map word and double-word cycles at any location to multiple byte reads or writes. The user should be aware that the MG-1's 32000 processor places the least significant byte of a word or double-word lowest in memory; this convention is the same for the Intel processors used on IBM PCs.

I/O — There are two sets of MG-1 locations which are mapped into the PC bus' 64k IO space. The lower set should be used for all processor accesses to IO registers; an address in the upper set is decoded by the bus adapter to mean that a PC bus DMA cycle should be simulated. See the section below on DMA programming.

4. Interrupt Assignments

The bus adapter has a patch-panel which can be used to select which of six PC bus interrupts, plus IO_CH_CK, are connected to up to the five MG-1 hardware interrupt levels reserved for the bus adapter. Default connections are as follows:

PC bus signal	MG-1 level
IRQ2	2
IRQ3	5
IRQ4	7
IRQ5	9
IRQ6	12
IRQ7	no connection
IO_CH_CK	no connection

5. DMA service

One fully-programmable DMA channel in the MG-1 is available for servicing the PC bus, performing DMA cycles whenever

triggered by an IBM PC boards DRQ signal. One of four DMA devices is selected by a subchannel number in a programmable latch; channel 3 is for the on-board floppy disc controller, and channels 0-2 correspond to the three DRQ/DACK pairs on the PC bus, as follows:

MG1 subchannel	IBM-PC DRQ/DACK No
0	3
1	2
2	1

The latch is programmed by writing a byte to hex FFE200; the bottom two bits are the DMA subchannel, but bit 2 must always be set 1 (if zero, the DRAM is disabled!).

Some features of DMA cycles on the PC bus are handled by special MG-1 hardware:

DACK IBM PC DMA cycles use the DACK signal as a data strobe for the card. Accesses to the "DMA" area of the PC bus adapters memory map will generate an appropriately-timed DACK strobe; the exact location addressed within the DMA page will be unimportant.

TC The 8037's TC signal can be used by a device to detect the last cycle of a DMA transfer. In the MG-1 the timing of this signal, which is a little odd, is generated by a separate programmable counter.

Standard DMA access routines are provided in the MG-1 Unix kernel; device drivers should always use these because they manage the sharing of the DMA channel between devices, and program the bus adapter to emulate IBM PC DMA cycles.

The I/O channel is an extension of the 8088 microprocesso[illegible]. It is, however, demultiplexed, repowered, and enhanced by the addition of interrupts and Direct Memory Access (DMA) functions.

The I/O channel contains an 8-bit bidirectional data bus, 20 address lines, 6 levels of interrupt, control lines for memory and I/O read or write, clock and timing lines, 3 channels of DMA control lines, memory refresh timing control lines a channel check line, and power and ground for the adapters. Four voltage levels are provided for I/O card +5 Vdc, -5 Vdc, +12 Vdc, and -12 Vdc. These functions are provided in a 62-pin connector with 100 mil card tab spacing.

A ready line is available on the I/O channel to allow operation with slow I/O or memory devices. If the channel's Ready line is not activated by an addressed device, all processor generated memory read and write cycles take four 210 ns clock or 840 ns/byte. All processor-generated I/O read and write cycles require five 210 ns clocks or 1.05 m sec/byte. All DMA transfers require five clocks for a cycle time of 1.05 m sec/byte. Refresh cycles are present once every 72 clocks or approximately 15 m sec and require five clocks or approximately 7% of the bus bandwidth.

I/O devices are addressed using I/O mapped address space. The channel is designed so that 512 I/O device addresses are available to the I/O channel cards.

A channel check line exists for reporting error conditions to the processor. Activating this line results in a NMI to the 8088 processor. Memory Expansion Options use this line to report parity errors

The I/O channel is repowered so there is sufficient drive to power all five System Expansion Slots, assuming two loads per slot. The IBM Option I/O adapters typically use only one load. A graphic illustration of the System I/O Channel and its descriptions are on the following pages.

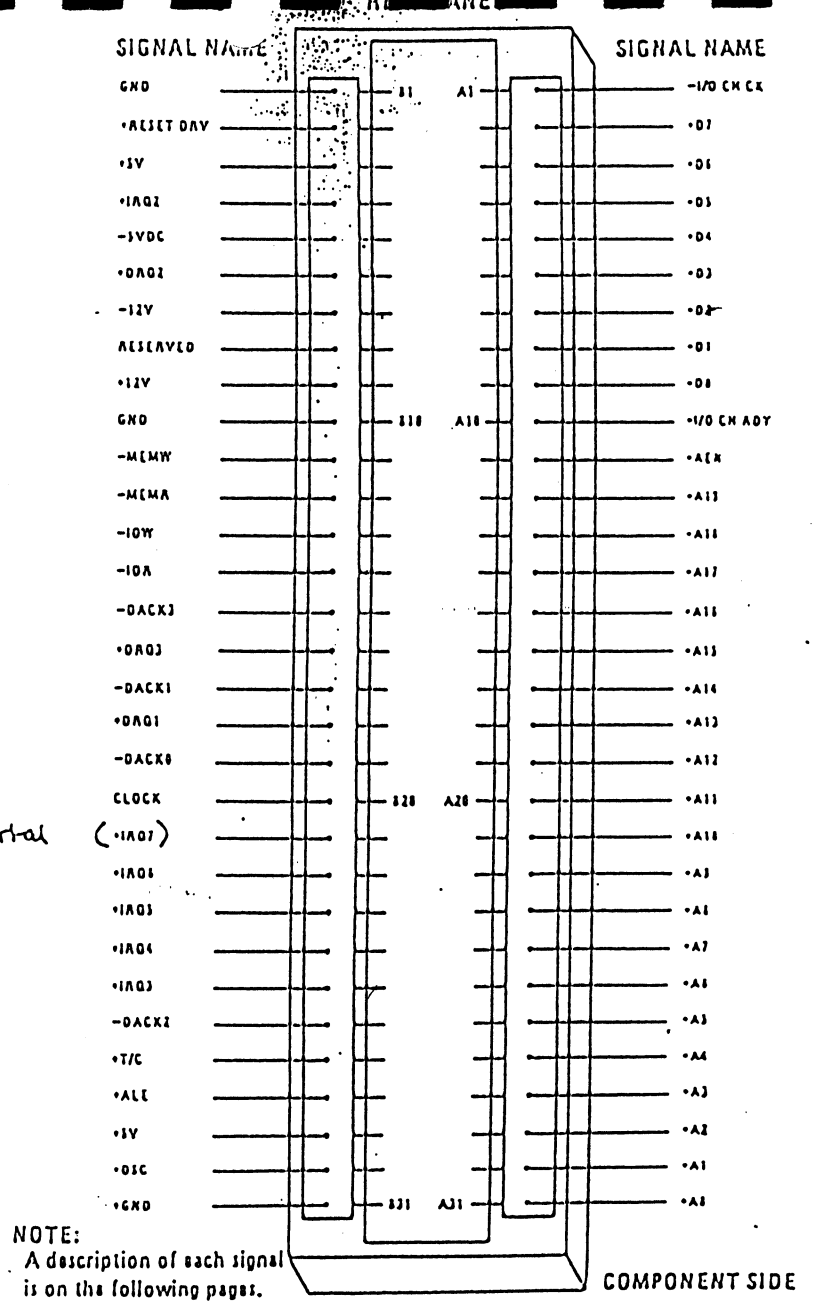


Figure 3. I/O CHANNEL DIAGRAM

Signal	I/O	Description
OSC	O	Oscillator: This signal is a high speed clock with a 70 nsec. period (14.31818 MHz). It has a 50% duty cycle.
CLK	O	Clock: This is the system clock. It is a divide - by - three of the oscillator and has a period of 210 nsec. (4.77 Mhz.) The clock has a 33% duty cycle.
RESET DRV	O	Reset Driver: This line is used to reset or initialize system logic upon power-up or during a low line voltage outage. This signal is synchronized to the falling edge of clock and is active HIGH.
A0-A19	O	Address Bits 0 to 19: These lines are used to address memory and I/O devices within the system. The 20 address lines allow access of up to 1 megabyte of memory. A0 is the Least Significant Bit (LSB) while A19 is the Most Significant Bit (MSB). These lines are generated by either the processor or the DMA Controller. They are active HIGH.
D0-D7	I/O	Data Bits 0 to 7: These lines provide data bus bits 0 to 7 for the processor, memory, and I/O Devices. D0 is the Least Significant Bit (LSB) and D7 is the Most Significant Bit (MSB). These lines are active HIGH.
ALE	O	Address Latch Enable: This is provided by the 8288 Bus Controller and is used on the System Board to latch valid addresses from the processor. It is available to the I/O Channel as an indicator of a valid processor address (when used in conjunction with AEN). Processor addresses are latched with the falling edge of ALE.
$\overline{\text{I/O CH CK}}$	I	-I/O Channel Check: This line provides the CPU with parity (error) information on memory or devices in the I/O Channel. When this signal is active LOW, a parity error is indicated.
		"High or "READY") is pulled low ("NOT "READY") by a memory or I/O device to lengthen I/O or memory cycles. It allows slower devices to attach to the I/O Channel with a minimum of difficulty. Any slow device using this line should drive it low immediately upon detecting a valid address and a Read or Write command. This line should never be held low for any period in excess of 10 clock cycles (2.1 usec.) Machine cycles (I/O or memory) are extended by an integral number of CLK cycles (210 ns).
IRQ2-IRQ7	I	Interrupt Request 2 to 7: These lines are used to signal the processor that an I/O device requires attention. They are prioritized with IRQ2 as the highest priority and IRQ7 as the lowest. An Interrupt Request is generated by raising an IRQ line (Low to High) and holding it high until it is acknowledged by the processor (Interrupt Service Routine).
$\overline{\text{IOR}}$	O	-I/O Read Command: This command line instructs an I/O device to drive its data onto the data bus. It may be driven by the processor or the DMA Controller. This signal is active LOW.
$\overline{\text{IOW}}$	O	-I/O Write Command: This command line instructs an I/O device to read the data on the data bus. It may be driven by the processor or the DMA Controller. This signal is active LOW.
$\overline{\text{MEMR}}$		-Memory Read Command: This command line instructs the memory to drive its data onto the data bus. It may be driven by the processor or the DMA Controller. This signal is active LOW.
$\overline{\text{MEMW}}$	O	-Memory Write Command: This command line instructs the memory to store the data present on the data bus. It may be driven by the processor or the DMA Controller. This signal is active LOW.

		DMA Request 1 to 3: These are asynchronous channel requests used by peripheral devices to gain DMA service. They are prioritized with DRQ1 having highest priority and DRQ3 the lowest. A request is generated by bringing a DRQ line to an active level (HIGH). A DRQ line must be held high until the corresponding DACK line goes active.
DACK0-DACK3	O	-DMA Acknowledge 0 to 3: These lines are used to acknowledge DMA requests (DRQ1-DRQ3) and to refresh system dynamic memory (DACK0). They are active LOW.
AEN	O	Address Enable: This line is used to degate the processor and other devices from the I/O Channel to allow Direct Memory Access (DMA) transfers to take place. When this line is active (HIGH), the DMA Controller has control of the address bus, data bus, read command lines, (memory and I/O), and the write command lines, (memory and I/O).
TC	O	Terminal Count: This line provides a pulse when the terminal count for any DMA channel is reached. This signal is active HIGH.

The following voltages are available on the System Board I/O Channel:

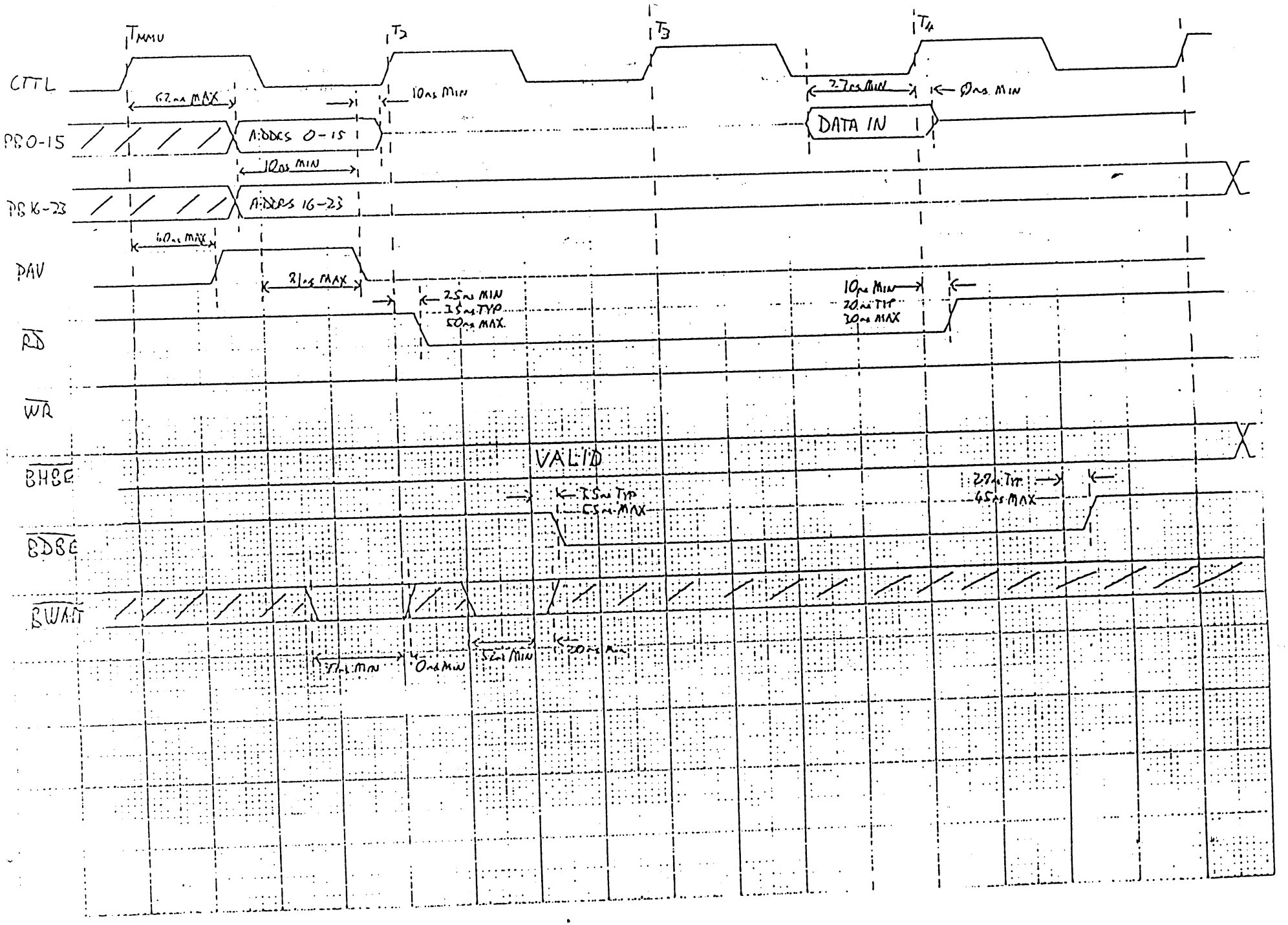
+5 Vdc ± 5%. Located on 2 connector pins.

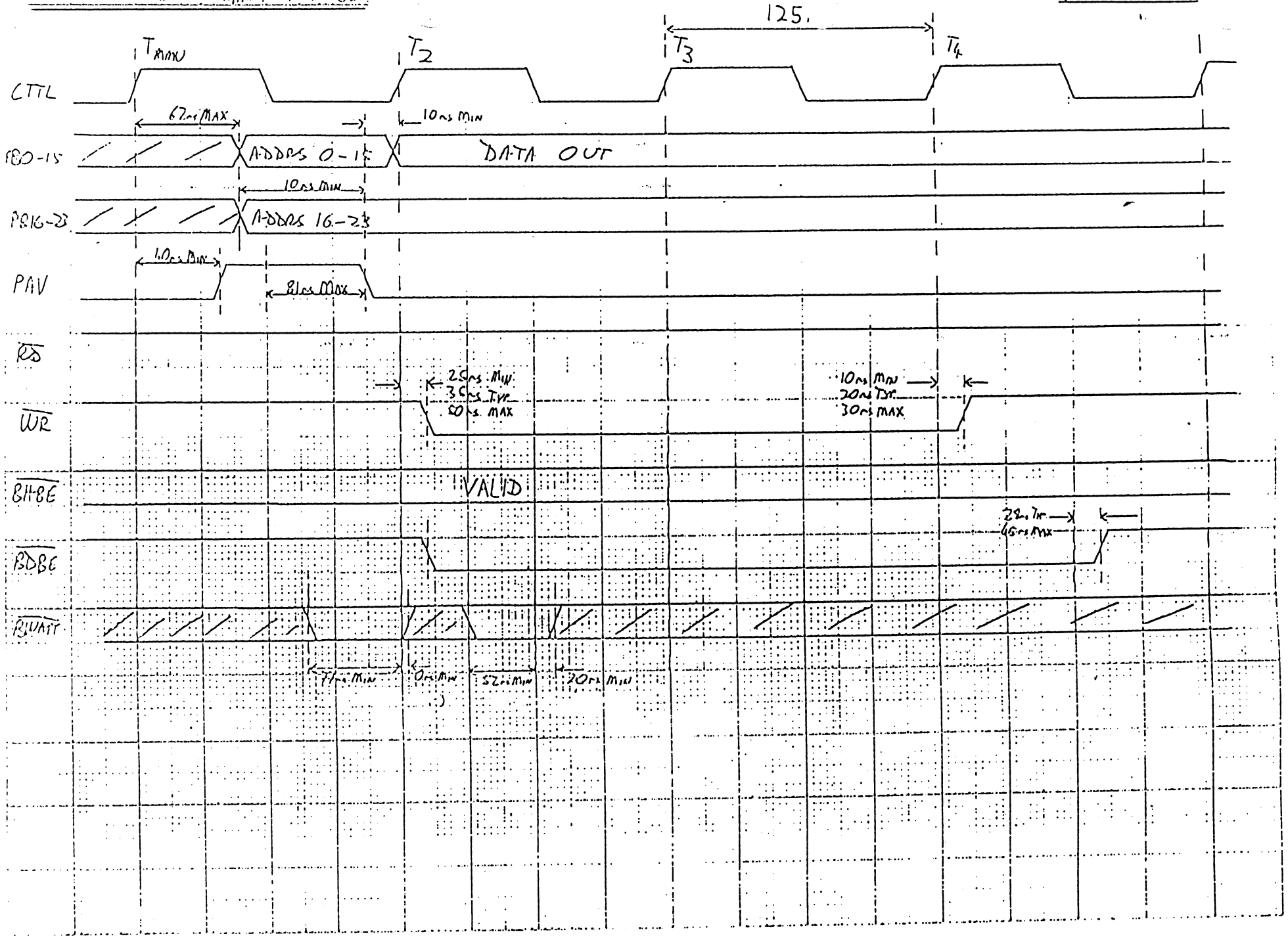
+5 Vdc ± 10%. Located on 1 connector pin.

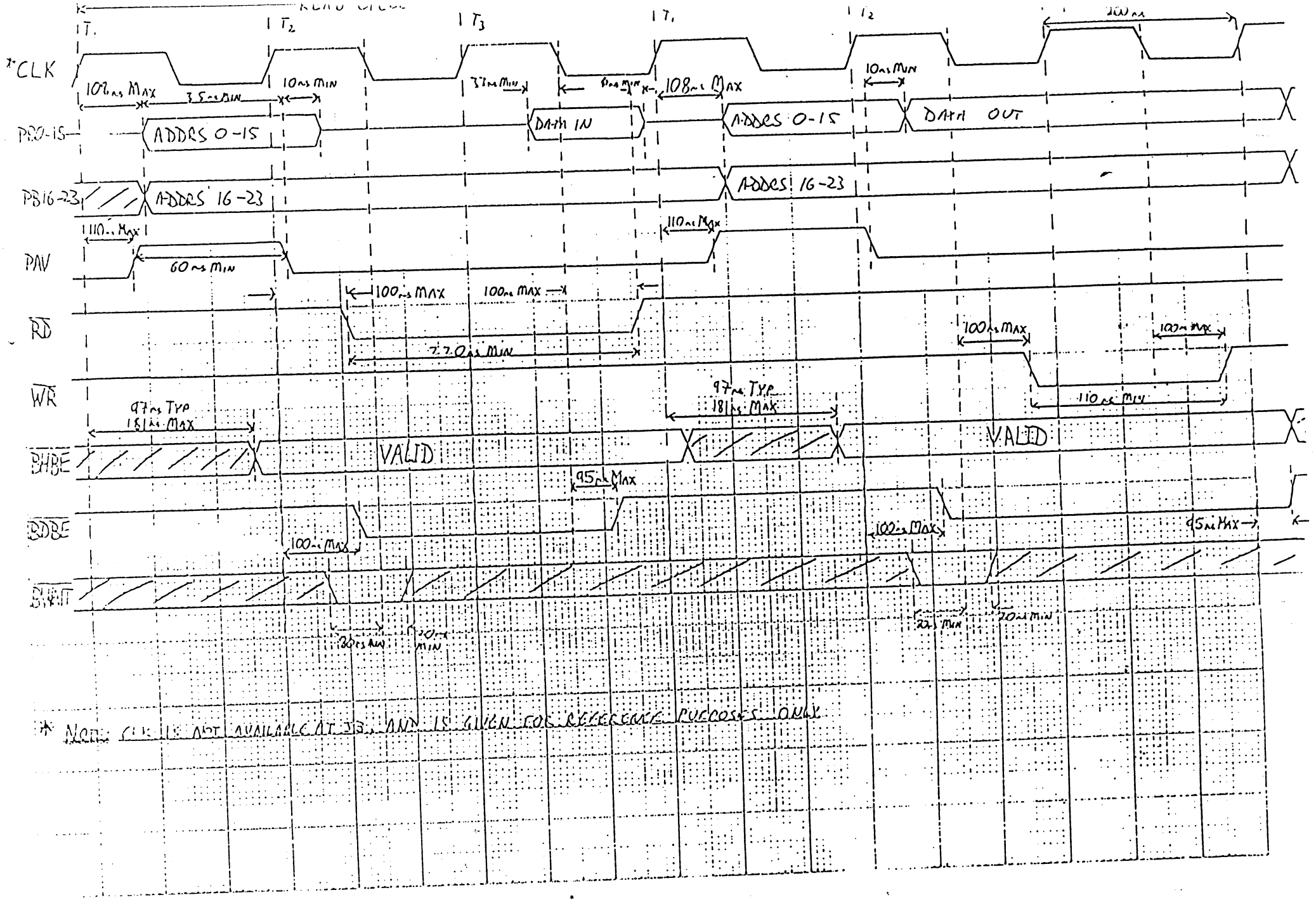
+12 Vdc ± 5%. Located on 1 connector pin.

-12 Vdc ± 10%. Located on 1 connector pin.

GND (Ground). Located on 3 connector pins.


T MMU
T2
T3
T4
CTTL
67ns MAX
10ns MIN
27.5ns MIN
0ns MIN
DATA IN
PB0-15
ADDRS 0-15
10ns MIN
PB16-23
ADDRS 16-23
40ns MIN
PAV
21ns MAX
2.5ns MIN
35ns TYP
50ns MAX
10ns MIN
20ns TYP
30ns MAX
RD
WR
VALID
BHBE
15ns TYP
65ns MAX
27ns TYP
45ns MAX
BDBE
BWAIT
37ns MIN
0ns MIN
52ns MIN
20ns MIN


125.
T1
T2
T3
T4
CTTL
62ns MAX
10ns MIN
AD0-15
ADDRS 0-15
DATA OUT
10ns MIN
AD16-23
ADDRS 16-23
10ns MIN
PAV
80ns MAX
RD
25ns MIN
35ns TYP
80ns MAX
10ns MIN
20ns TYP
30ns MAX
WR
BHBE
VALID
22ns TYP
45ns MAX
BDBE
BUSY
77ns MIN
0ns MIN
52ns MIN
20ns MIN


T1
T2
T3
T1
T2
*CLK
PA0-15
PB16-23
PAV
RD
WR
BHBE
BDBE
BWAIT
ADDRS 0-15
ADDRS 16-23
DATA IN
ADDRS 0-15
DATA OUT
ADDRS 16-23
VALID
VALID
60ns MIN
97ns TYP
181ns MAX
97ns TYP
181ns MAX
95ns MAX
95ns MAX
* NOTE: CLK IS NOT AVAILABLE AT J3, AND IS GIVEN FOR REFERENCE PURPOSES ONLY.

Support Bulletin: Accessing devices on the 'IBM' bus

Graham C Adams

distribution: ALL SERVICE STAFF

machine: MG-1

os: 42-nix 2.0

importance: handy-hints

problem:

Customers wish to access devices on the IBM PC compatible bus. Under 42-nix release 2.0 no code is provided to facilitate this.

notes:

There are two ways to access devices on the IBM bus.

The first is to access the device via a device driver built into the kernel. This will not be possible for customers who have only a binary license until release 2.5 of 42-nix is available. That release will support the addition of user written drivers.

The only way to access arbitrary devices at present is through the /dev/kmem device. This should be opened with the required read/write flags (see open(2)). To select an address lseek(2) should be used, the offset being the address required. Input and output may then be performed using the standard read(2) and write(2) functions. Note that reads and writes will increment the 'file pointer' i.e. the address, so to write to a single location a series of lseeks and 1 byte write operations will be necessary.

The base address of the IBM bus is at 0xd00000.
Access to addresses in the range 0xd00000 to 0xddffff results in normal memory cycles on the IBM bus (IBM addresses 00000 to dffff).

The base address for i/o transfers (simulated IBM i/o bus cycles) is 0xde0000. Thus IBM i/o address 0x3F8 would be accessed via 0xde03F8.

The base address for dma transfers is 0xdf0000.

SUPPORT NOTES NO. 14

a Non Standard Keyboard to the MG-1

The MG-1's 'D-connector' keyboard interface operates on the following pin allocations:

Pin 1: [not used]
Pin 2: Data from keyboard
Pin 3: Reset to keyboard
Pin 4: Ground (0v)
Pin 5: Power (+5v)

The interface is a standard asynchronous type configured for 1200 Baud, No parity, 8 bits data (bit 7 gives key UP/DOWN information), 1 start bit, 2 stop bits.

The keyboard scan codes are as shown in the accompanying diagram.

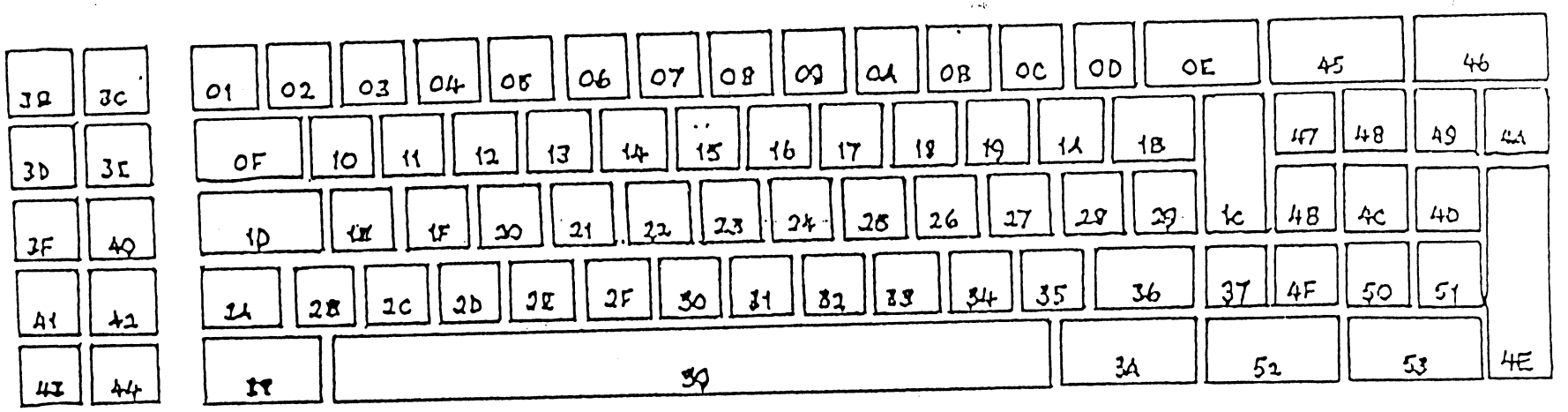
Any non-standard keyboard must generate the same UP/DOWN data as the MG-1 keyboard, and maintain the standard key repeat mechanism, i.e.,

1. Bit 7: 0 for downcode
   1 for upcode.

2. ALT, SHIFT, and CTRL should send a downcode when first depressed, then send an upcode when released.

3. NUMLOCK and CAPSLOCK should send a downcode when first depressed, then send an upcode when released. At power-up or reset, the NUMLOCK and CAPSLOCK LED's should switch off. These LED's should toggle on and off each time the key is used.

   The first time the key is rapidly depressed and released, as a single operation, the LED's should switch on. The second rapid depression/release should switch them off. This cycle must repeat.


3B
3C
01
02
03
04
05
06
07
08
09
0A
0B
0C
0D
0E
45
46
3D
3E
0F
10
11
12
13
14
15
16
17
18
19
1A
1B
47
48
49
4A
3F
40
1D
1C
1E
20
21
22
23
24
25
26
27
28
29
1C
4B
4C
4D
41
42
2A
2B
2C
2D
2E
2F
30
31
32
33
34
35
36
37
4F
50
51
43
44
1F
39
3A
52
53
4E

SUPPORT NOTES NO. 15

MG-1 Maintenance Procedure

1. Unplug MG-1 and remove mains power lead.

2. Unscrew upper sleeve and slide forward, [Fig 1]. Lay the sleeve behind the unit. Note that there is an earthing lead attached to the inner surface of the sleeve.

3. Unscrew the earthing lead from the inner surface of the sleeve. Note that this lead is attached to the Power Distribution Board. It should not be unscrewed at this end, [Fig 2].

4. Remove the short black power lead from the rear of the Floppy Disk Drive. Note that this lead is plugged into the Power Distribution Board on the right hand side, [Figs 2 & 6].

5. Slide the earthing lead out of the rear of the Floppy Disk Drive. The earth should not be unscrewed from the PDB, [Fig 2].

6. Remove the long black power lead from the rear of the Winchester Drive. It need not be disengaged from the PDB, [Figs 2 & 6].

7. Slide the earthing lead out of the rear of the Winchester Drive. The earth should not be unscrewed from the PDB, [Figs 2 & 6].

8. Unplug the 34-way ribbon cable from the rear of the Floppy Disk Drive. At this stage, do not attempt to remove the ribbon cables from the unit completely, [Fig 2].

9. Unplug the 34- and 20-way ribbon cables from the rear of the Winchester Drive, [Fig 2].

10. Unplug the 11-pin cable assembly from the PDB. Note that this cable is wired into the Power Supply Board, and cannot be disengaged at this end, [Figs 2 & 6].

11. Unplug the 3-pin cable assembly from the PDB. This cable is also wired into the Power Supply Board, and cannot be removed, [Figs 2 & 6].

12. Unplug the black power lead from the underside of the fan unit, [Fig 3].

13. Unscrew the earth lead from the top of the fan unit, [Fig 3].

14. Unscrew the earth lead from the rear panel of the chassis, [Fig 3].

15. Unscrew the earth lead from the support strut of the upper tray. Note that these leads should not be unscrewed from the PDB, [Fig 3].

16. Unscrew the upper tray from the chassis, [Fig 7].

17. Unscrew the Power Distribution assembly from the rear panel of the chassis, [Fig 3].

18. Lift out the upper tray assembly and remove the PBD. Take care when disengaging the lower edge of the PDB from the pins on the main board, [Fig 6].

19. Unscrew the front panel board, and lift out. Take care when disengaging the lower edge of the board from the main board pins, [Fig 5].

20. Unscrew the rear moulding panel.

21. Unscrew the fan unit from the rear panel of the chassis, [Fig 3].

22. Remove the ribbon cables from the main board.

23. Unscrew the D-plug connectors from the rear panel of the chassis and from the main board. Lift out the port plates, [Fig 4].

24. Untie and remove the DMA Piggy Board.

25. Remove the MMU Piggy Board, where present.

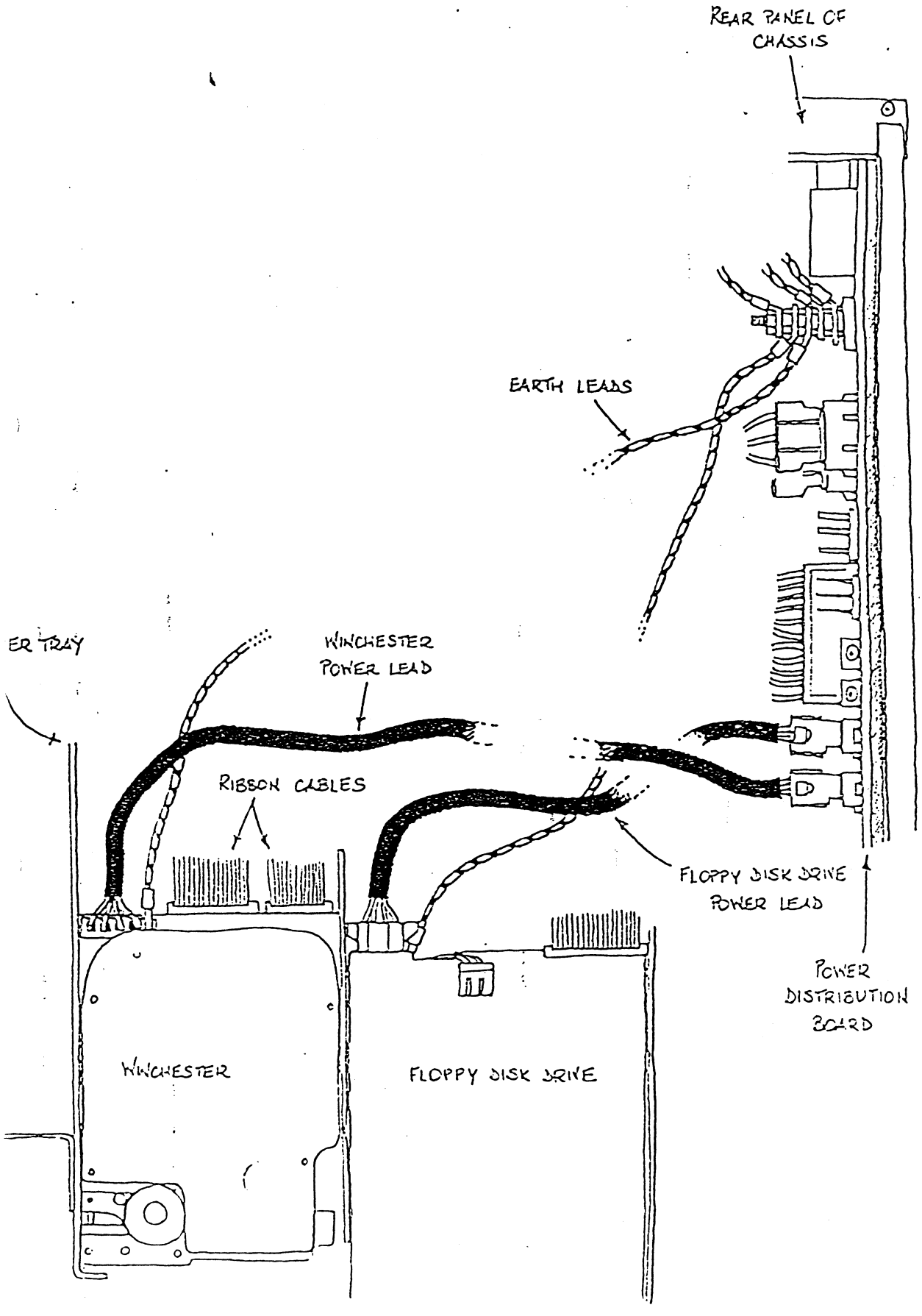
26. Unscrew the nylon separator posts holding in the Memory Expansion Cards, where present. Lift off the top card, taking care not to damage the pins connecting the card to the card below or to the main board. Repeat.

27. Remove the remaining nylon posts, and lift out the Main Board, [Fig 6].

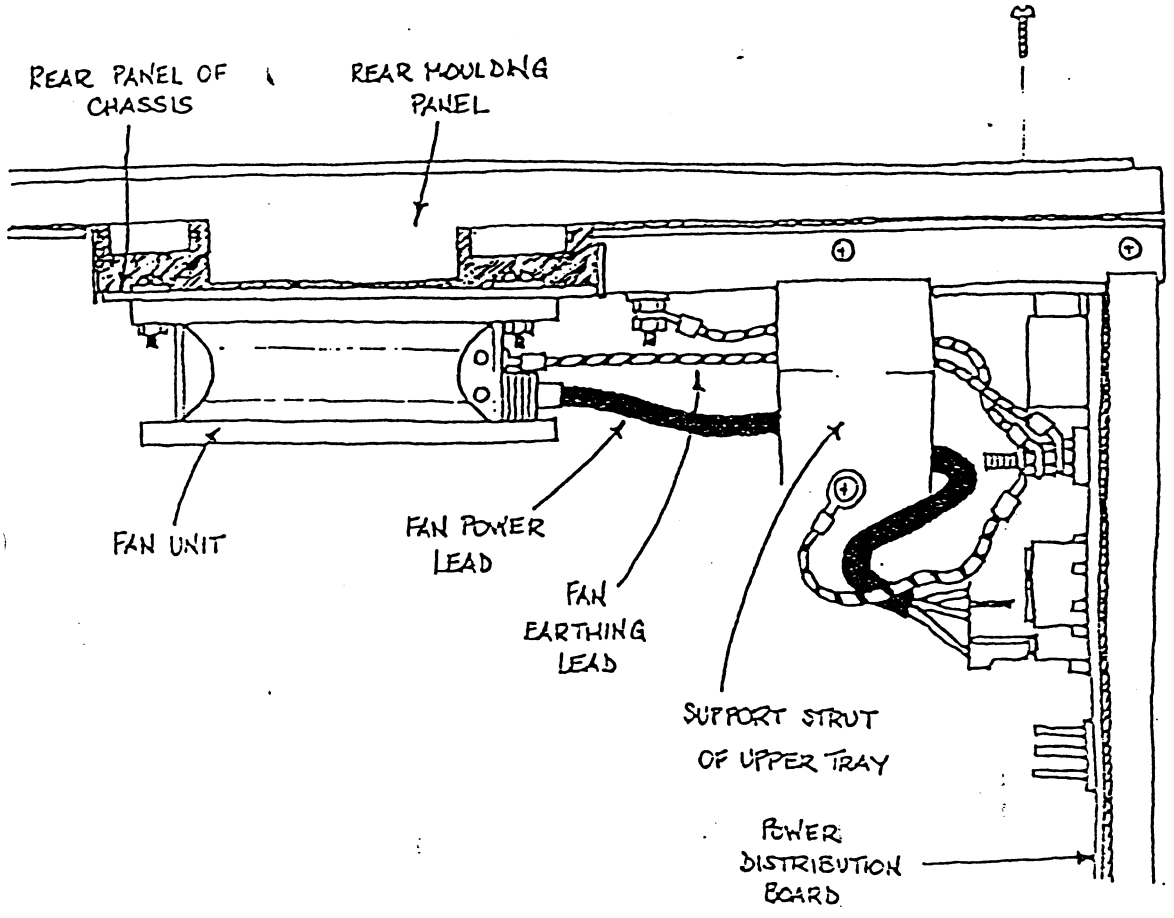
28. To dismantle the top tray assembly, begin by removing the two screws along the right hand side of the Floppy Disk Drive. Slide out the drive unit, [Fig 7].

29. Remove the four retaining screws from the sides of the Winchester Drive, and slide out the unit, [Fig 7].

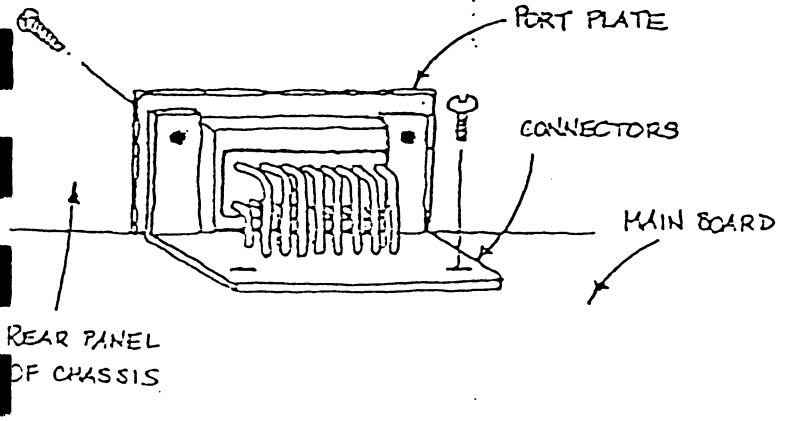
30. To remove the Power Supply Board, push back the nylon retainers at the four corners, and lift out of the tray. The retainers may be left in place, [Fig 7].



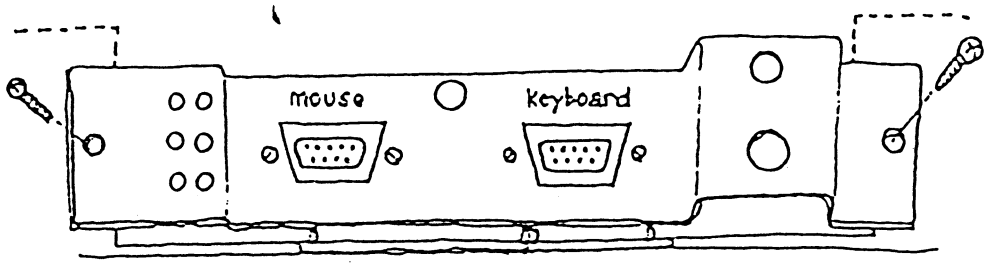
DISENGAGING THE DISK DRIVES FROM THE POWER SUPPLY



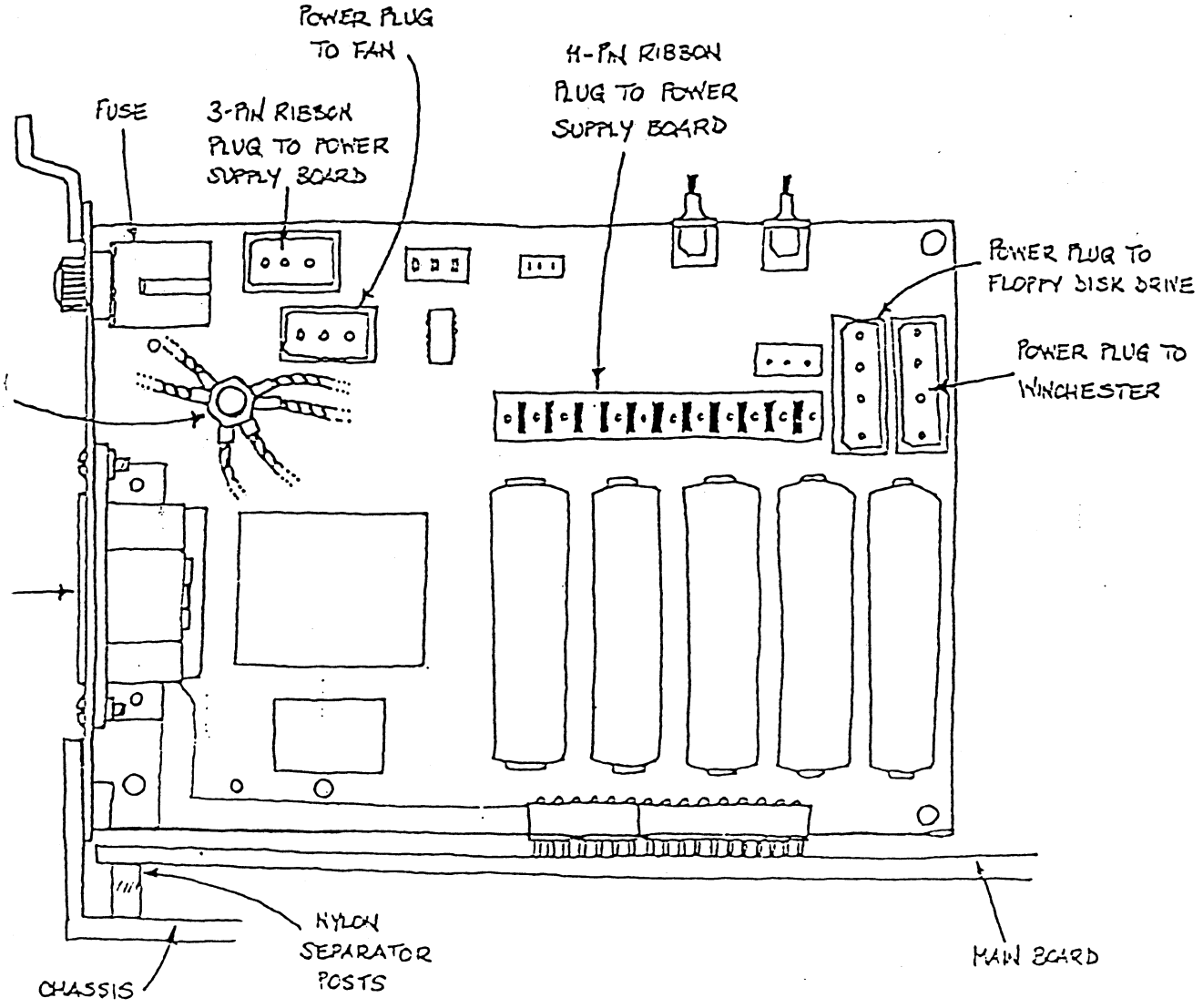
DISENGAGING THE FAN UNIT AND CHASSIS EARTH LEADS.



4. 5-PLUG CONNECTORS.



THE FRONT PANEL



E POWER DISTRIBUTION BOARD.

MG-1 Main Board Pin Assignments.

J1 Pin Assignments.

Front Panel Connection: 24-pin SIL MOLEX connector, series 4030. Pins are on an 0.1" pitch as shown:

1 2 3 4 5 . . . . . 22 23 24

as seen from the component side of the PCB.

Pin	
1	0v
2	0v
3	+5v
4	+5v
5	FP-RESET/
6	N.C
7	ON_SW
8	XA
9	XB
10	YA
11	YB
12	N.C
13	BUTTON0
14	BUTTON1
15	BUTTON2
16	Fault code LED
17	Speaker
18	KBRD-DATA
19	KRBD-CLK
20	N.C
21	+5v
22	+5v
23	0v
24	0v

J2 Pin Assignment.

Ethernet Connection: 15-pin male `D' pin connector with slide lock assembly. Pins are not on a 0.1" pitch grid, but are arranged as follows:

```
      15   14   13   12   11   10   9
    8    7    6    5    4    3    2    1
```

as seen from the component side of the PCB.

Pin		Pin	
1	0v	9	Collision Present -
2	Collision Present +	10	Transmit -
3	Transmit +	11	
4		12	Receive -
5	Receive +	13	+12v
6		14	
7		15	
8			

J3 Pin Assignments.

Expansion Bus Connection: 64-pin DIL female Eurocard DIN type connector. The pins are on a 0.1" pitch grid, as shown:

```
Row B  1 2 3 4 5 . . . . . . . . 32
Row A  1 2 3 4 5 . . . . . . . . 32
```

as seen from the component side of the PCB.

Row A		Row B	
1	0v	1	0v
2	+5v	2	+5v
3	+12v	3	+12v
4	0v	4	0v
5	N.C	5	N.C
6	CTTL	6	IO_PAGE/
7	PAV	7	ST1
8	BDBE	8	BHBE/
9	BWAIT	9	EOP/ (IBM TC)
10	RQ1/	10	ACK1/
11	RQ2/	11	ACK2/
12	RQ3/	12	ACK3/
13	RD/	13	WR/
14	BUS_INT2/	14	BUS_INT3/
15	BUS_INT4/	15	BUS_INT5/
16	BUS_INT6/	16	RESET
17	N.C	17	N.C
18	PB0	18	PB1
19	PB2	19	PB3
20	PB4	20	PB5
21	PB6	21	PB7
22	PB8	22	PB9
23	PB10	23	PB11
24	PB12	24	PB13
25	PB14	25	PB15
26	PB16	26	PB17
27	PB18	27	PB19
28	PB20	28	PB21
29	PB22	29	PB23
30	N.C	30	-12v
31	+5v	31	+5v
32	0v	32	0v

J4 Pin Allocations.

Modem Connection: 25-pin male `D' connector with slide lock assembly. Right angle PCB mounting version. Pins are not on a 0.1" pitch grid, but are arranged as shown:

```
  25  24  23  22  21  20  19  18  17  16  15  14
13  12  11  10   9   8   7   6   5   4   3   2   1
```

as seen from the component side of the PCB.

Pin		Pin
1	0v	14
2	TxD/	15
3	RxD/	16
4	RTS/	17
5	CTS/	18
6	DSR/	19
7	0v	20
8		21
9		22
10	DTR/	23
11		24
12		25
13		

26th Sept 1985

J3 Expansion Slot User Notes

Phil Martin

ABSTRACT

This set of notes is designed to give enough information to the user so that custom hardware may be designed that interfaces directly with the MG1 J3 expansion slot, rather than with the IBM Expansion bus. A description of all the pins on the connector is given, as well as timing diagrams for CPU & UDC read/write cycles.

November 4, 1985

J3 Expansion Slot User Notes

Phil Martin

1. Introduction

J3 provides a means of expanding the MG-1's capabilities - it is primarily intended to be used with the WCW IBM PC Motherboard, however, with this document it should be possible for users to design their own hardware to utilise it.

2. J3 Pin Outs:

J3 consists of a 64-pin DIL female Eurocard DIN type connector. The pins are on a 0.1" pitch as shown :-

Row B : 1 2 3 4 5 . . . . . 30 31 32

Row A : 1 2 3 4 5 . . . . . 30 31 32

As seen from the component side of the PCB

2.1. Pin Labelling

	Row A	Row B
1	0V	0V
2	+5V	+5V
3	+12V	+12V
4	0V	0V
5	N.C.	N.C.
6	CTTL	N.C.
7	PAV	ST1
8	BDBE/	BHBE/
9	BWAIT/	EOP/
10	RQ1/	ACK1/
11	RQ2/	ACK2/
12	RQ3/	ACK3/
13	RD/	WR/
14	BUS-INT2/	BUS-INT3/
15	BUS-INT4/	BUS-INT5/
16	BUS-INT6/	RESET
17	N.C.	N.C.
18	PB0	PB1
19	PB2	PB3
20	PB4	PB5
21	PB6	PB7
22	PB8	PB9
23	PB10	PB11
24	PB12	PB13
25	PB14	PB15
26	PB16	PB17
27	PB18	PB19
28	PB20	PB21
29	PB22	PB23
30	N.C.	-12V
31	+5V	+5V
32	0V	0V

3. Pin Descriptions

3.1. Power Lines & Unused Pins

- GND (Pins 1A, 1B, 4A, 4B, 32A, 32B) - Ground
- +5V (Pins 2A, 2B, 31A, 31B) - +5V @ ...
- +12V (Pins 3A, 3B) - +12V @ ...
- -12V (Pin 30A) - -12V @ ...
- N.C. (Pins 5A, 5B, 6B, 17A, 17B, 30A) - No connection

3.2. Input Signals

- RQ1/, RQ2/, RQ3/ (Pins 10A, 11A, 12A) - DMA Request lines. Active Low. Connected to the DREQ2/ input of UDC #2. Only one RQn/ line may be active at one time - selection is made by writing the number of the request line OR'ed with 0x04 to DMASBASE (0x0ffe200). Request line zero is reserved for the MG-1 internal floppy disk drive.

- BUS-INT2/- BUS-INT6/ (Pins 14A, 14B, 15A, 15B, 16A) - Bus interrupt request lines. Active Low. Connected to system ICU (NS32202) as follows:-

Interrupt Line	ICU Pin
BUS-INT2/	IR2
BUS-INT3/	IR5
BUS-INT4/	IR7
BUS-INT5/	IR9
BUS-INT6/	IR12

- BWAIT/ (Pin 9A) - Wait Input. Active Low. Used to extend control signals when dealing with slow memory & peripheral devices. If used, this line should be driven by an open-collector output.

3.3. Output Signals

- RESET (Pin 16B) - Reset Output Signal. Active High.

- PB16-23 (Pins 26A - 29B) - Processor Bus 16 - 23. Active High. These are the buffered most significant 8 bits of the memory address bus, as generated by the CPU & UDCs.

- PAV (Pin 7A) - Physical Address Valid. Active High. Controls address latches.

- CTTL (Pin 6A) - TTL System Clock. This is a TTL output version of PHI1. Therefore, it operates at the CPU clock frequency.

- BDBE/ (Pin 8A) - Buffered Data Bus Enable. Active Low. This signal is used to enable or tri-state buffers on the system data lines. It is low when the buffers are to be enabled.

- BHBE/ (Pin 8B) - Buffered High Byte Enable. Active Low. Status signal enabling transfer of data on the most significant byte of the Data Bus.

- RD/ (Pin 13A) - Read Output Strobe. Active Low. Identifies a read cycle.

- WR/ (Pin 13B) - Write Output Strobe. Active Low. Identifies a write cycle.

- ACK1/, ACK2/, ACK3/ (Pins 10B, 11B, 12B) - DMA acknowledges. Active Low. Connected to the DACK2/ line of UDC #2. Acknowledges are sent to the currently active channel corresponding to the RQn/ line that requested the DMA.

- ST1 (Pin 7B) - CPU Status line 1. This signal is provided to allow additional ICU's to be cascaded onto the system ICU. Connecting this signal to the ST1 input on a cascaded ICU allows it to distinguish between an Interrupt Acknowledge cycle and an End Of Interrupt cycle.

- EOP/ (Pin 9B) - End Of Process for IBM PC Motherboard. Active low. This signal is designed to simulate the timing of the 8237 DMA Controller EOP/ signal when the MG-1 is performing DMA operations via the IBM PC Motherboard.

3.4. Input/Output Signals

- PB0-15 (Pins 18A - 25B) Address/Data lines 0 - 15. Active High. Multiplexed Address/Data information. Bit 0 is the least significant bit of each. For DMA transactions, MG-1 circuitry 'byte-reverses' the data to/from the UDCs so that the byte on PB0-7 is the least significant, as with CPU transactions.

J5 Pin Assignments.

Monitor Signal Connection: 15-pin female 'D' connector with slide lock assembly. Right angle PCB mounting version. Pins are not on a 0.1" pitch grid, but are arranged as shown:

```
        9   10   11   12   13   14   15
    1.   2    3    4    5    6    7    8
```

as seen from the component side of the PCB.

Pin		Pin	
1	0v	9	VIDEO/
2	VIDEO	10	0v
3	VSYNC – 57Hz	11	VSYNC/
4	0v	12	HSYNC/
5	HSYNC – 47kHz	13	0v
6	DISP_EN	14	DISP_EN/
7	VMONITOR	15	VMONITOR
8	VMONITOR		

J6 Pin Assignments.

Winchester Data Signals: 20-pin DIL unshrouded header on a 0.1" pitch grid as shown:

```
2 4 6 8  . . . 20
1 3 5 7  . . . 19
```

as seen from the component side of the PCB.

Pin		Pin	
1	DRIVE_SELECTED/	2	0v
3		4	0v
5		6	0v
7		8	0v
9		10	0v
11	0v	12	0v
13	MFM_WRITE_DATA	14	MFM_WRITE_DATA
15	0v	16	0v
17	MFM_READ_DATA	18	MFM_READ_DATA
19	0v	20	0v

J7 Pin Assignments.

Winchester Control Signals: 34-pin DIL unshrouded header on a 0.1" pitch grid, as shown:

```
2 4 6 8 . . . . . 34
1 3 5 7 . . . . . 33
```

as seen from the component side of the PCB.

Pin		Pin	
1	0v	2	REDUCED_WRITE_CURRENT/
3	0v	4	HEAD_SELECT_2/
5	0v	6	WRITE_GATE/
7	0v	8	SEEK_COMPLETE/
9	0v	10	TRACK_0/
11	0v	12	WRITE_FAULT/
13	0v	14	HEAD_SELECT_0/
15	0v	16	
17	0v	18	HEAD_SELECT_1/
19	0v	20	INDEX/
21	0v	22	READY/
23	0v	24	STEP/
25	0v	26	DRIVE_SELECT_1/
27	0v	28	+5v
29	0v	30	+5v
31	0v	32	+5v
33	0v	34	DIRECTION_IN/

J8 Pin Assignments.

Floppy Disk Signals: 34-pin DIL unshrouded header on a 0.1" pitch grid as shown:

```
2 4 6 8 . . . . . 34
1 3 5 7 . . . . . 35
```

as seen from the component side of the PCB.

Pin		Pin	
1	0v	2	
3	0v	4	HEAD_SELECT/
5	0v	6	
7	0v	8	INDEX_PULSE/
9	0v	10	0v
11	0v	12	0v
13	0v	14	0v
15	0v	16	MOTOR_ON/
17	0v	18	DIRECTION/
19	0v	20	STEP/
21	0v	22	WRITE_DATA/
23	0v	24	WRITE_GATE/
25	0v	26	TRACK_00/
27	0v	28	WRITE_PROTECT/
29	0v	30	READ_DATA/
31	0v	32	
33	0v	34	

J9 Pin Assignments.

Power Connection: 24-pin SIL MOLEX connector, series 4030.
Pins are on a 0.1" pitch as shown:

```
     1
     2
     3

     .
     .
     .

     24
```

as seen from the component side of the PCB.

Pin	
1	0v
2	0v
3	+5v
4	+5v
5	+5v
6	0v
7	VMONITOR
8	VMONITOR
9	VMONITOR
10	-12v
11	ON_SW
12	RST_SW/
13	NMI_SW/
14	POWER_FAIL/
15	VBACKUP
16	0v
17	+12v
18	+12v
19	0v
20	+5v
21	+5v
22	+5v
23	0v
24	0v

J10 Pin Assignments.

Memory Bus (Low Bytes): 64-pin DIL female Eurocard DIN type connector. The pins are on a 0.1" pitch grid as shown:

Row A	Row B
1	1
2	2
3	3
.	.
.	.
32	32

as seen from the component side of the PCB.

Row A		Row B	
1	0v	1	0v
2	+5v	2	+5v
3	BHBE/	3	BUS_CYCLE/
4	N.C	4	WR/
5	CAS_TIME/	5	LLA0
6	LLA1	6	LLA2
7	UPPER_MADR0	7	UPPER_MADR1
8	UPPER_MADR2	8	UPPER_MADR3
9	UPPER_MADR4	9	N.C
10	WD0	10	WD1
11	WD2	11	WD3
12	WD4	12	WD5
13	WD6	13	WD7
14	0v	14	0v
15	0L0 (MRD0)	15	1L0 (MRD16)
16	0L1 (MRD1)	16	1L1 (MRD17)
17	0L2 (MRD2)	17	1L2 (MRD18)
18	0L3 (MRD3)	18	1L3 (MRD19)
19	0L4 (MRD4)	19	1L4 (MRD20)
20	0L5 (MRD5)	20	1L5 (MRD21)
21	0L6 (MRD6)	21	1L6 (MRD22)
22	0L7 (MRD7)	22	1L7 (MRD23)
23	2L0 (MRD32)	23	3L0 (MRD48)
24	2L1 (MRD33)	24	3L1 (MRD49)
25	2L2 (MRD34)	25	3L2 (MRD50)
26	2L3 (MRD35)	26	3L3 (MRD51)
27	2L4 (MRD36)	27	3L4 (MRD52)
28	2L5 (MRD37)	28	3L5 (MRD53)
29	2L6 (MRD38)	29	3L6 (MRD54)
30	2L7 (MRD39)	30	3L7 (MRD55)
31	+5v	31	+5v
32	0v	32	0v

J11 Pin Assignments.

Memory Bus (High Bytes): 64-pin DIL female Eurocard DIN type connector. The pins are on a 0.1" pitch grid as follows:

Row A	Row B
1	1
2	2
3	3
.	.
.	.
32	32

as seen from the component side of the PCB.

Row A		Row B	
1	0v	1	0v
2	+5v	2	+5v
3	0H0 (MRD8)	3	1H0 (MRD24)
4	0H1 (MRD9)	4	1H1 (MRD25)
5	0H2 (MRD10)	5	1H2 (MRD26)
6	0H3 (MRD11)	6	1H3 (MRD27)
7	0H4 (MRD12)	7	1H4 (MRD28)
8	0H5 (MRD13)	8	1H5 (MRD29)
9	0H6 (MRD14)	9	1H6 (MRD30)
10	0H7 (MRD15)	10	1H7 (MRD31)
11	2H0 (MRD40)	11	3H0 (MRD56)
12	2H1 (MRD41)	12	3H1 (MRD57)
13	2H2 (MRD42)	13	3H2 (MRD58)
14	2H3 (MRD43)	14	3H3 (MRD59)
15	2H4 (MRD44)	15	3H4 (MRD60)
16	2H5 (MRD45)	16	3H5 (MRD61)
17	2H6 (MRD46)	17	3H6 (MRD62)
18	2H7 (MRD47)	18	3H7 (MRD63)
19	0v	19	0v
20	WD8	20	WD9
21	WD10	21	WD11
22	WD12	22	WD13
23	WD14	23	WD15
24	U_MUX_MADR0	24	U_MUX_MADR1
25	U_MUX_MADR2	25	U_MUX_MADR3
26	U_MUX_MADR4	26	U_MUX_MADR5
27	U_MUX_MADR6	27	U_MUX_MADR7
28	U_MUX_MADR8	28	CLOSE_CYCLE/
29	U_RAS0/	29	U_RAS1/
30	U_RAS2/	30	U_RAS3/
31	+5v	31	+5v
32	0v	32	0v

SUPPORT NOTES NO. 20

Information on the Depraz Mouse

depraz mouse

DEPRAZ S A

MANUFACTURED BY DEPRAZ SA
CH 1345 LE LIEU
SWITZERLAND

1. Principle : - Mechanical tracking with opto-électronic decoding
   - Quadrature outputs signals
   - 3 debounced push buttons

2. Mechanical specifications :
   - Dimensions : 90 x 73 x 45
   - Weight : 160 gr. with cable and connector
   - Case : fire proosing plastic (makrolon)
   - Cable : 9 conductor 47", unshielded (shielded cable optional)
   - Termination : subminiatur Cannon 9 P male (9 P female optional)
   - Ball Stainless steel, diameter 20 mm removable for easy cleaning.

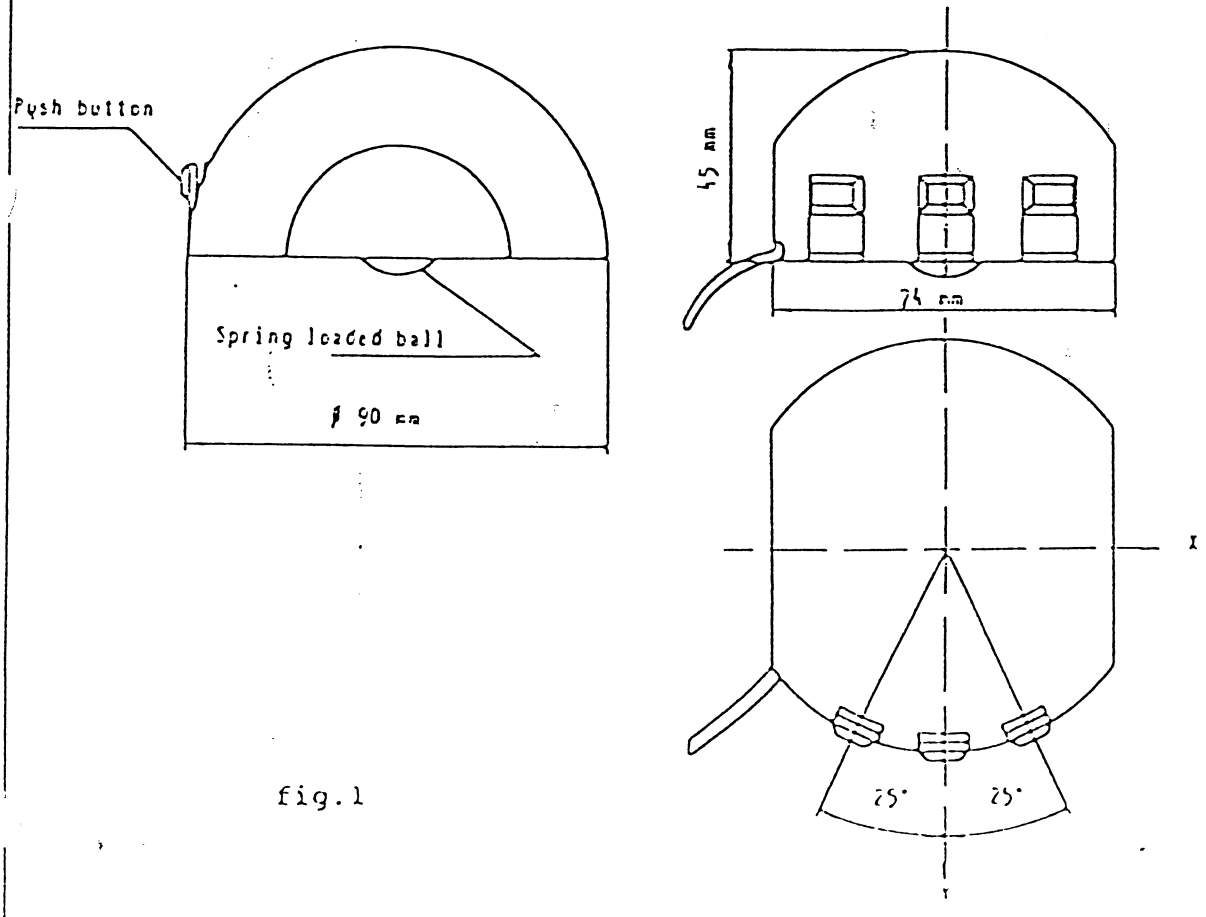


fig.1

DEPRAZ - MOUSE D 83 / P and D 83 / H

The mouse has been shown to be an ideal interactive input device for computer graphics, word processing and office automation applications. Several products use a mouse successfully, and many personal workstations under development in various research projects have selected this input device for efficient man-machine dialogue.

The principle of the mouse is to encode and transfer to the computer the displacement of the mouse held in the palm of the hand, which can rest comfortably on the table next to the keyboard. Three keys easity depressed by the fingers can trigger a particular action or set a particular mode of operation in interaction with the display program.

A Swiss product

The Dépraz-Mouse D 83 features improved performance and better ergonomical shape at a lower price. Two models exist : type P with a parallel interface and type H with signal serialisation. Industrial manufacturing starced early in 1982 by a competent company next to the Lac de Joux (50' from Genève-Cointrin).

General description

The hemispherical shape (diameter 90 mm) of the mouse is easily grasped by the hand, with the three middle digits laying on the keys while the thumb and the little finger move the mouse precisely in interaction with the display. A plain tactile feedback is felt while depressing any key, and the way the mouse is held prevents any movement while depressing a key. (fig. 1)

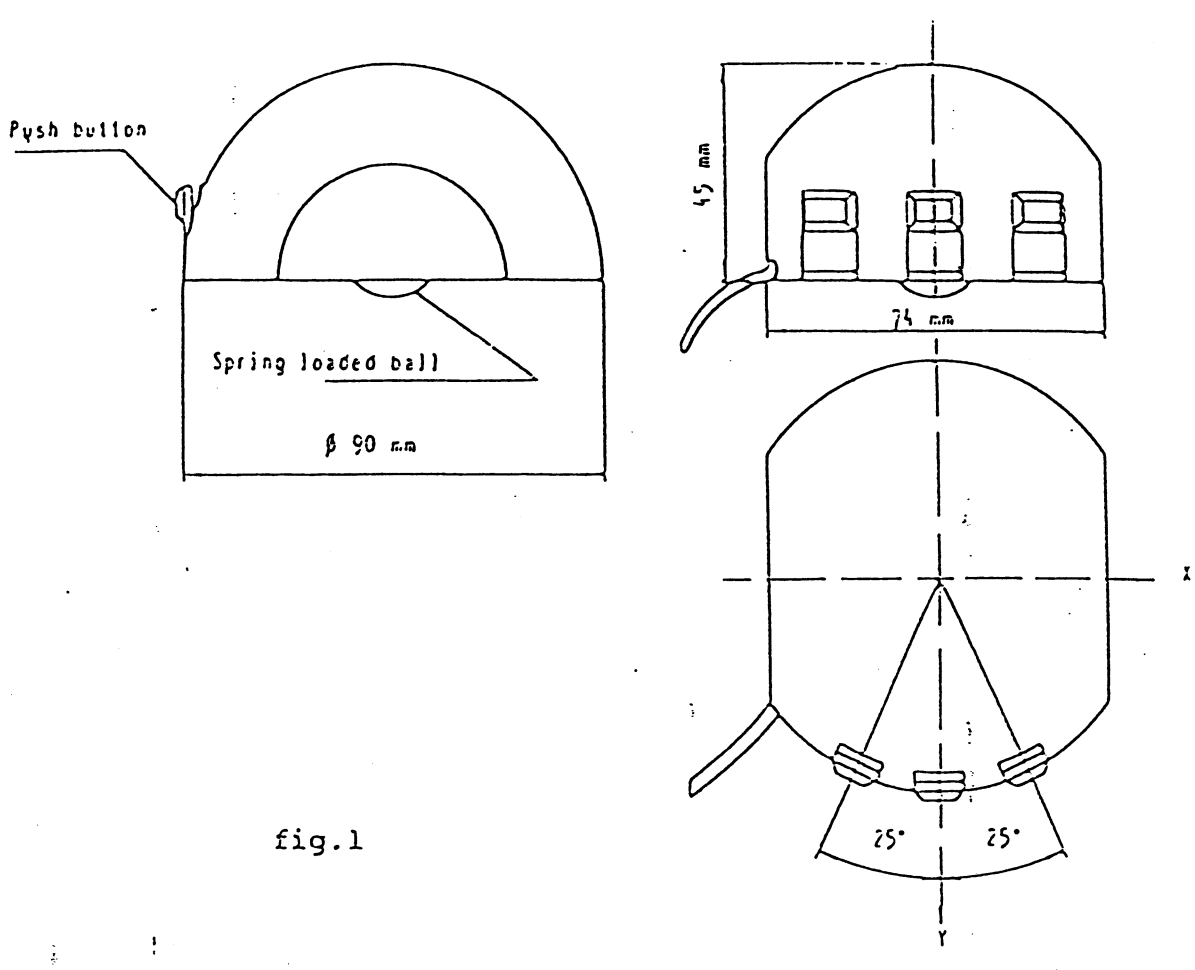
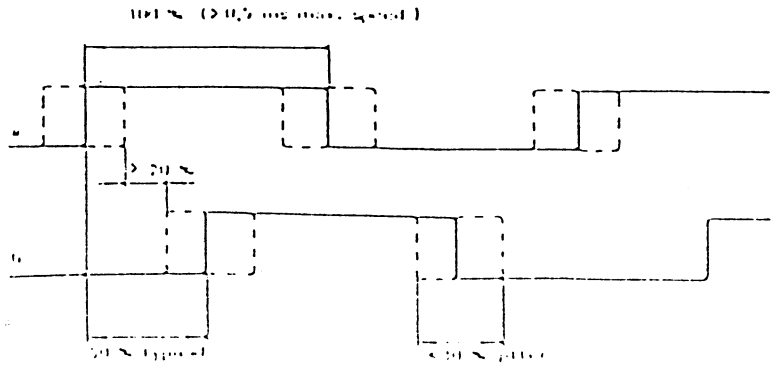


fig.1

As the mouse is moved over the table top, a steel rolling pin of 20 mm diameter rotates. This rotation is decomposed into two perpendicular axes. For each axis, two square signals are produced, out of phase by 90 degrees, providing 15 pulses per millimeter, at any speed the hand can produce. Alignment and jitter is such that distance between consecutive pulses is guarantied. Pulse generation rate at maximum hand speed is about 1 ms (fig. 2).



The mouse is usually held so that the X-axis is parallel to the major axis of the axis of the wrist,but the user can find any position that is comfortable.The Y-axis is perpendicular to the X-axis.

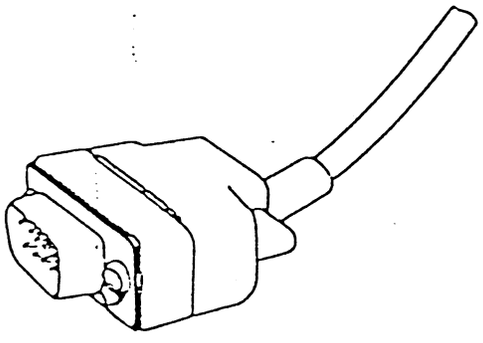
If the number of 15 pulses per mm is too high for standard applications, it can be easily divided by hardware or software.

Precision optical wheels with phototransistors and Schmitt trigger generate the signals.

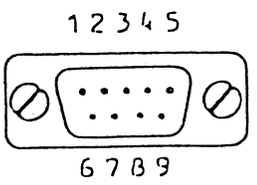
On the standard mouse type P, 4 lines carry the pulses out of the mouse through a 9 wires cable which also carry the status of the three switches, the power supply (+ 5V ± 10 %) and the power and signal return line (GND). The mouse D 83,type H shifts the 7 bits information through a 5 lines cable including the power supply.Power consumption is 40 mA.
All signals are CMOS and TTL-LS compatible.

MOUSE D 83/P

Standard connector on P4 is a male 9 pins Cannon subminiature connector (fig.3).An 120 cm long (4 feet).
Cable is provided.



Cannon 2 DE 9P connector
Symbol on schematic



Male plug
front view

Pin 1	+ 5V	6	GND
2	y2	7	$\overline{H}$
3	y1	8	$\overline{D}$
4	x2	9	$\overline{C}$
5	x1		

fig.3

The mouse is usually held so that the X-axis is parallel to the major axis of the axis of the wrist,but the user can find any position that is comfortable.The Y-axis is perpendicular to the X-axis.

If the number of 15 pulses per mm is too high for standard applications, it can be easily divided by hardware or software.

Precision optical wheels with phototransistors and Schmitt trigger generate the signals.

On the standard mouse type P, 4 lines carry the pulses out of the mouse through a 9 wires cable which also carry the status of the three switches, the power supply (+ 5V ± 10 %) and the power and signal return line (GND). The mouse D 83,type H shifts the 7 bits information through a 5 lines cable including the power supply.Power consumption is 40 mA.
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MOUSE D 83/P

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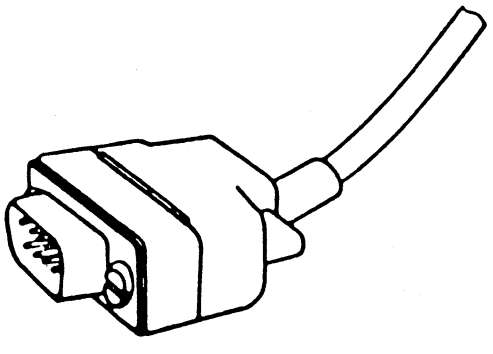
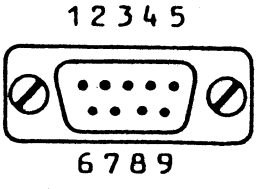


Cannon 2 DE 9P connector
Symbol on schematic



Male plug
Front view

Pin 1 + 5V	6 GND
2 y2	7 $\overline{M}$
3 y1	8 $\overline{D}$
4 x2	9 $\overline{G}$
5 x1	

fig.3

The D 83 / P mouse schematic is given in figure 4. When a key is depressed, the corresponding output is active low.

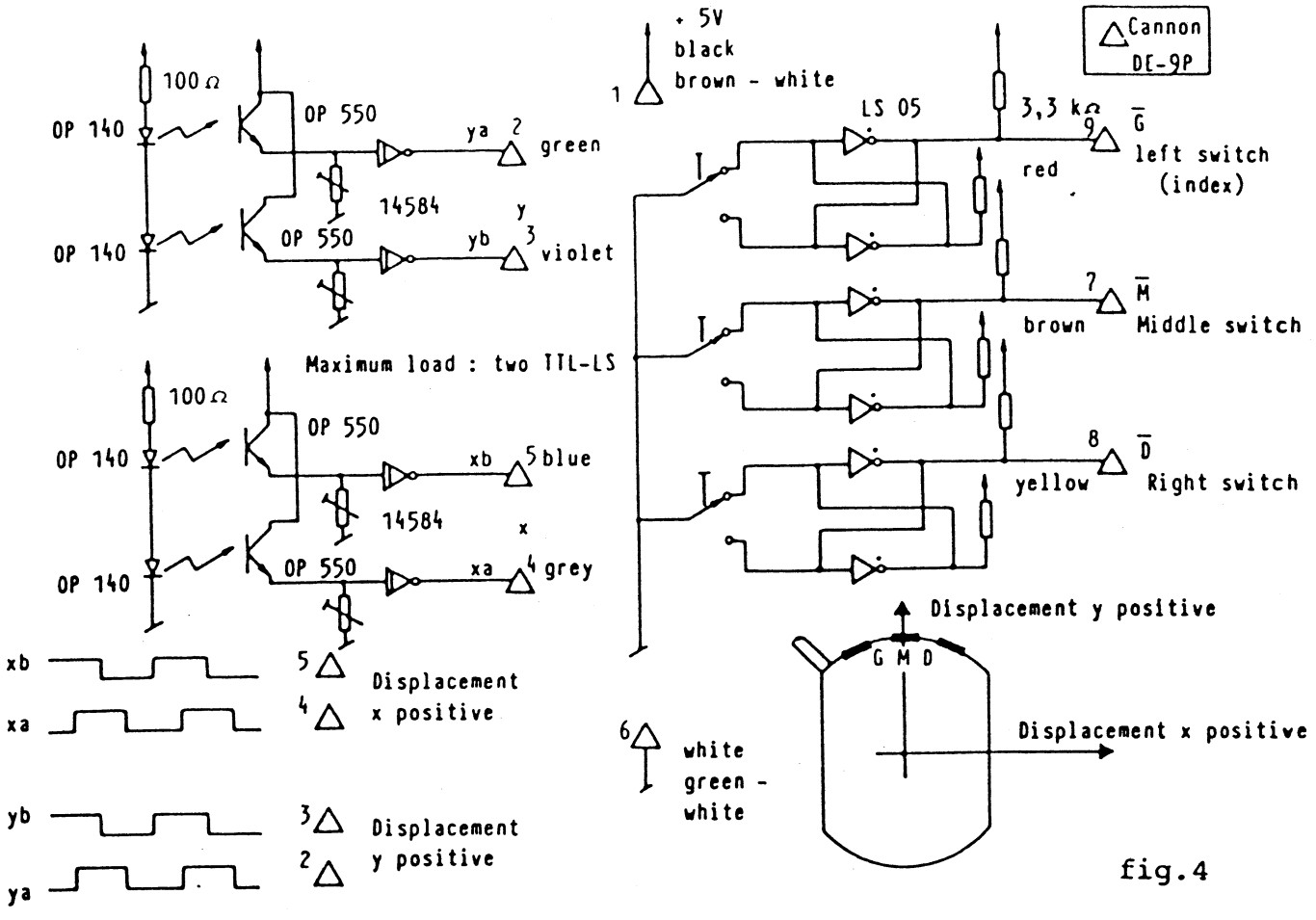


fig.4

APPLICATION NOTE

Interfacing the mouse D 83 / P is easy. The three switches can be directly read on a parallel port and scanned by software. If handling by interrupt is required, a 3-input or gate can trigger an interrupt when any key is depressed. Two 2-input exclusive OR gate plus two flip-flops can trigger an interrupt each time a key is pressed or depressed (see figure 5).

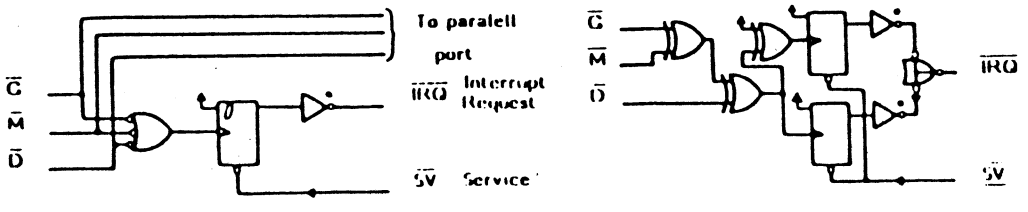


fig.5

The D 83 / P mouse schematic is given in figure 4. When a key is depressed, the corresponding output is active low.

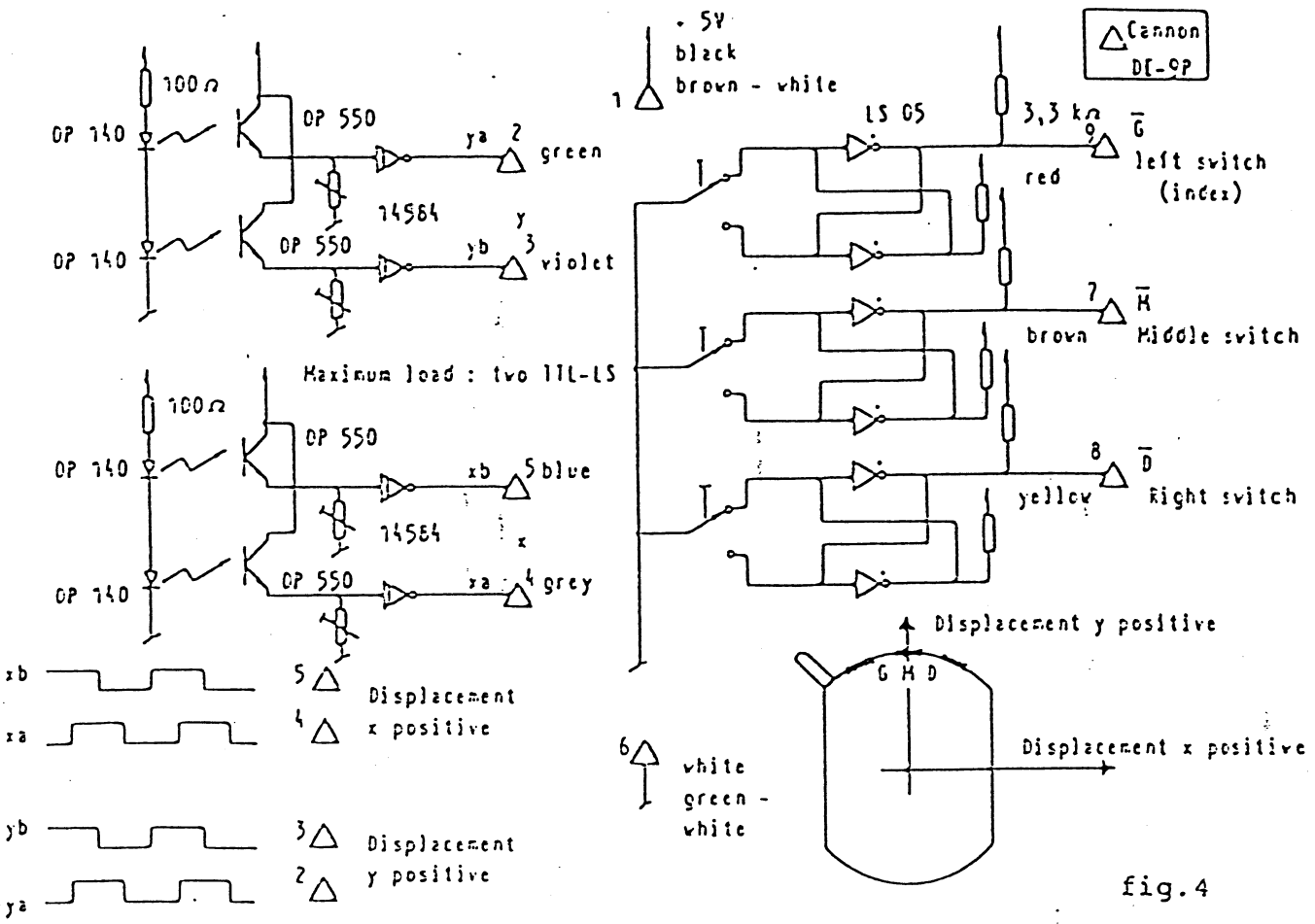


fig.4

APPLICATION NOTE

Interfacing the mouse D 83 / P is easy. The three switches can be directly read on a parallel port and scanned by software. If handling by interrupt is required, a 3-input or gate can trigger an interrupt when any key is depressed. Two 2-input exclusive OR gate plus two flip-flops can trigger an interrupt each time a key is pressed or depressed (see figure 5).

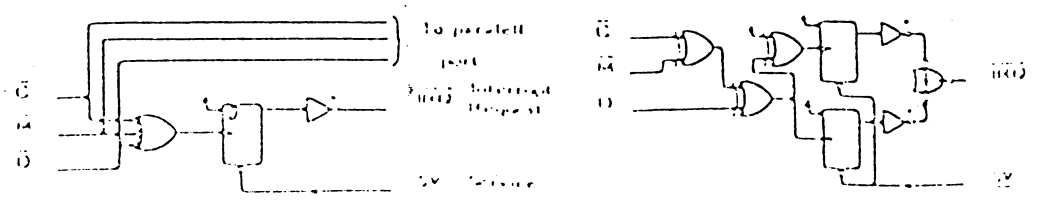


fig.5

The four pulse lines control an up-down counter which can be hardware, or programmed. If made in hardware, the counter will by read regulary to update the pointer on the screen. If made in software, interrupts will occur each time a pulse is decoded.

Decoding of the pulses can be made with different schematics, depending on the required resolution.

One pulse per period

Fig. 6 shows a simple schematic, which in most cases is quite adequate with the number of pulses per millimetre provided by the mouse. Direction is defined from the value of "b" at each positive pulse edge of "a", and a delayed pulse is generated for the up-down counters at each positive "a" transition.

The delayed negative pulse is required with counters made of pulse-tripped master-slave flip-flops like the 74LS190/191. With these counters, UP/DOWN state must not be changed while the clock is active low.

If the counter is updated by an interrupt routine, two flip-flops provide the required interface (fig. 6c). In a microprocessor system, a better choice than the LS191 is a LS697, which provides a three-state buffer and a latch (fig. 7). An AND gate inhib the load of the register when the register is read by the microprocessor, in order to avoid any change of state while reading.

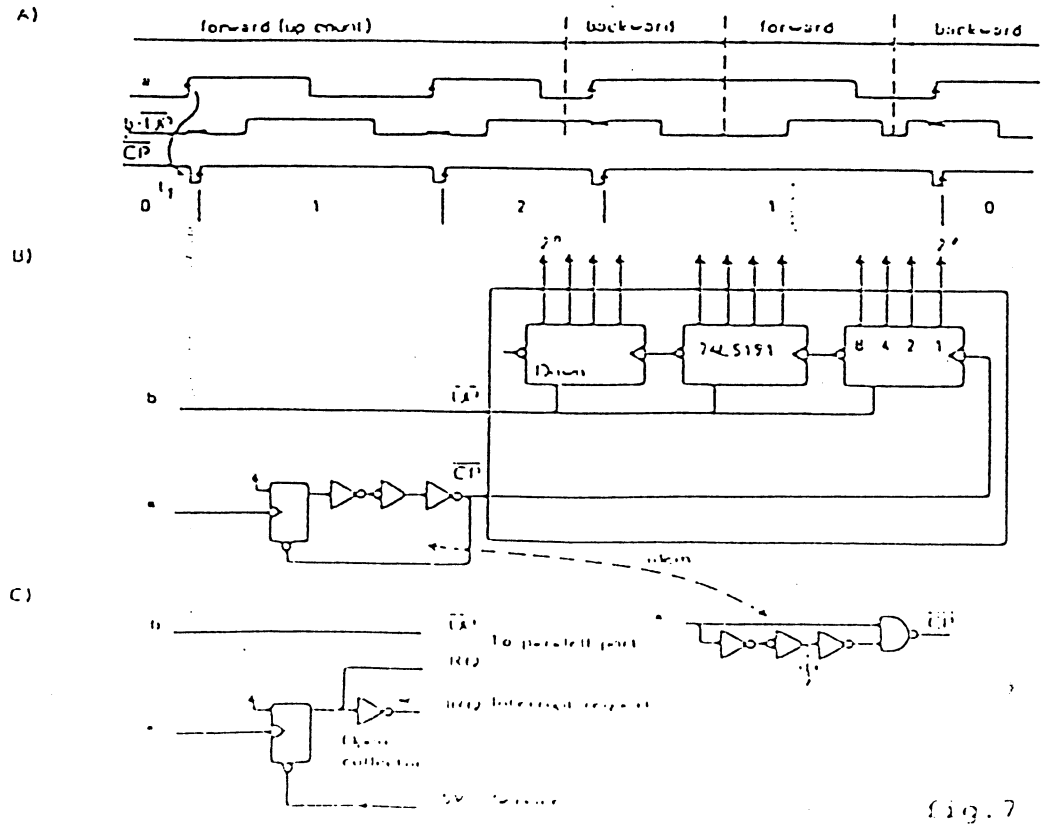


fig. 7

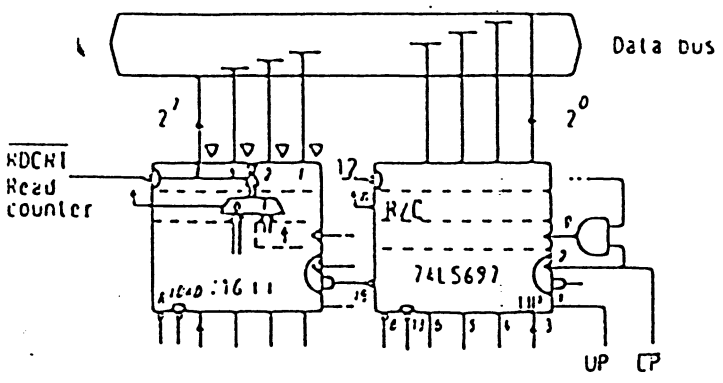


fig.7 Microprocessor interface with three-state up-down counters

A better approach is in most cases to use a programmable timer/ counter like the 8253, 6840 or 9513. Two channels have to be used in order to simulate an up/down counter by subtraction (fig.8).

Two pulses per period

Both pulse edges of signal "a" can be used for an improved resolution. The corresponding timing diagram and schematic is given in fig.8. In this schematic, generation of delays and pulses of adequate length rely on the mixing of CMOS and TTL-LS technology. If all CMOS technology must be used, or if programmable timer have to be used, additional delays must be provided inside the dotted schematic regions.

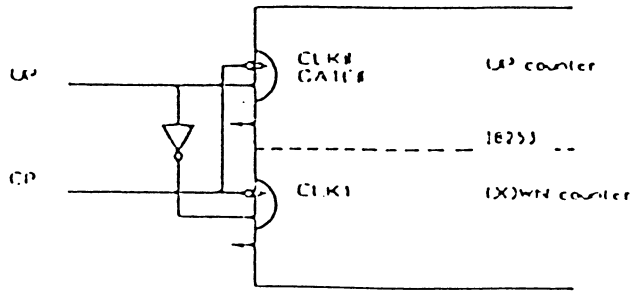


fig.8

A purely synchronous solution with clocked flip-flops for the generation of delays is shown in figure 10. There is a risk for metastable states, but due to the rather slow clock (100 kHz range, one can neglect this risk. Loosing a pulse every month is acceptable with a mouse.

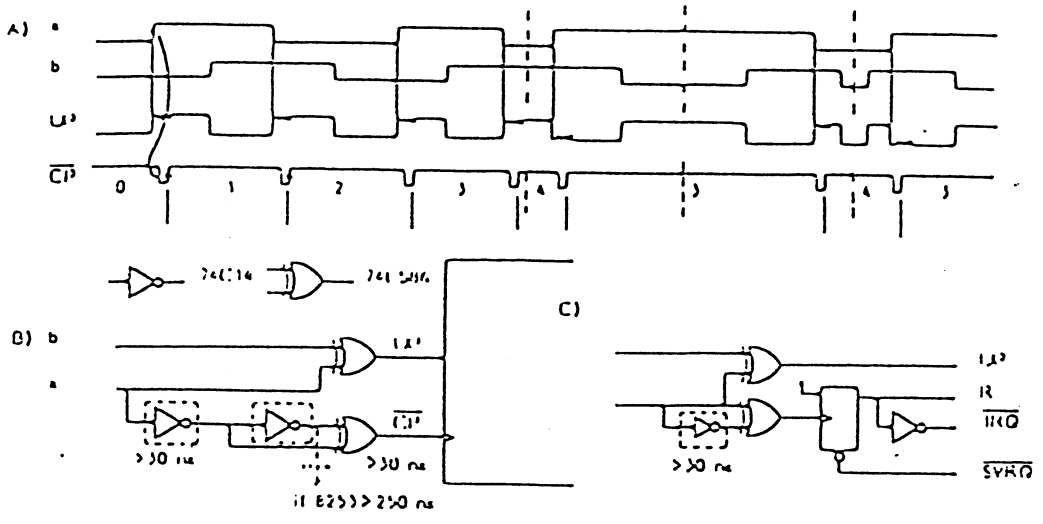


fig.9 Interface with 2 counts per pulse

A) Timing diagramm

B) Schematic for hardware counter

C) Schematic with interrupts and software counters

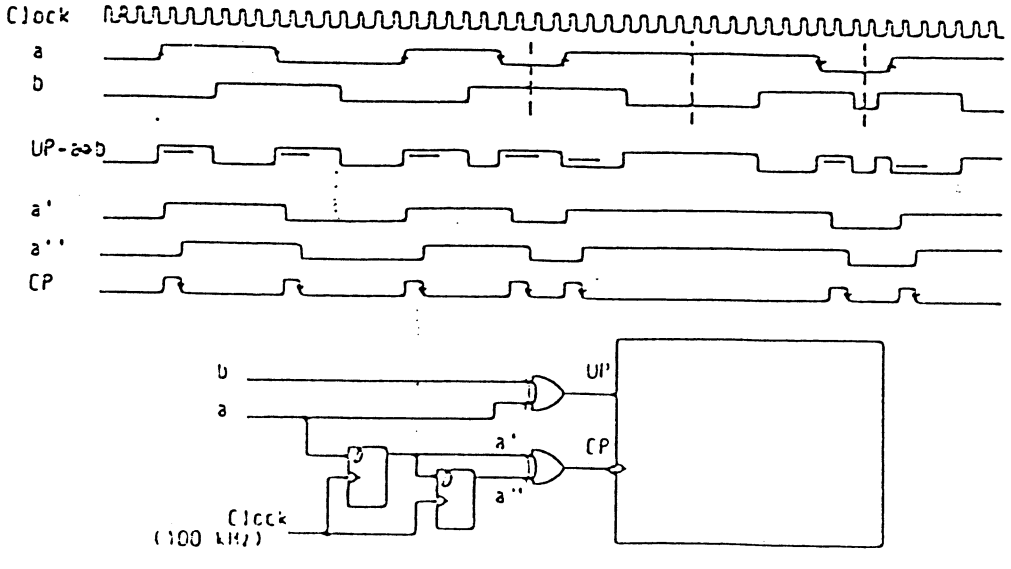


fig.10 Synchronous interface with two counts per pulse

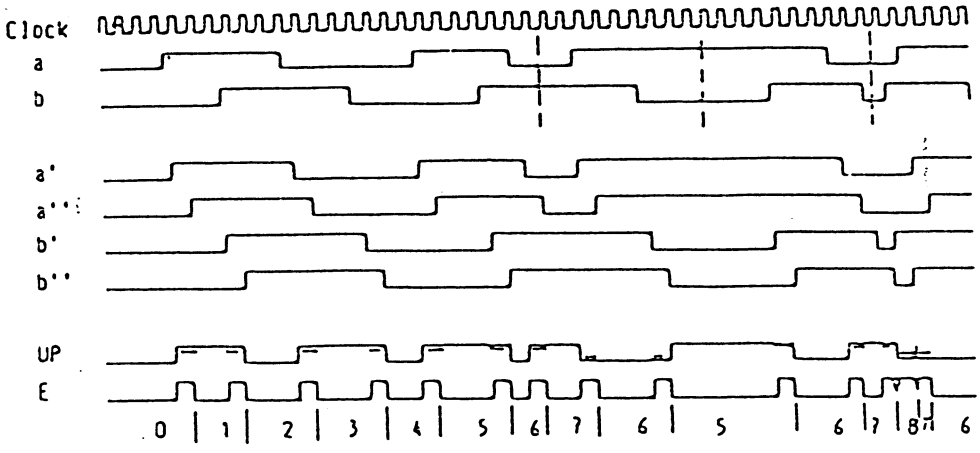
A) Timing diagram

B) Schematic with hardware counter

3. Four pulses per period

The highest resolution is obtained with 4 pulses per period. The synchronous schematic of fig.11 generalizes the previous scheme. The LS174 or LS175 register (LS273 for two channels) generates delayed pulses whith defines the count slots (enable the counter) and the direction. The truth table is given in fig. 11b and assumes that the synchronizing clock is fast enough to nerer have two transitions in the same slot. CMOS technology can be used for lower power consumption.

A PROM can be used as shown in fig.11, but this increases the power and the cost for the saving of a single chip. A registered PROM or PAL can save an additional circuit.



b''	b'	a''	a'	E	UP
0	0	0	0	0	-
0	0	0	1	1	0
0	0	1	0	1	1
0	0	1	1	0	-
0	1	0	0	1	1
0	1	0	1	-	-
0	1	1	0	-	-
0	1	1	1	1	0
1	0	0	0	1	0
1	0	0	1	-	-
1	0	1	0	-	-
1	0	1	1	1	1
1	1	0	0	0	-
1	1	0	1	1	1
1	1	1	0	1	0
1	1	1	1	0	-

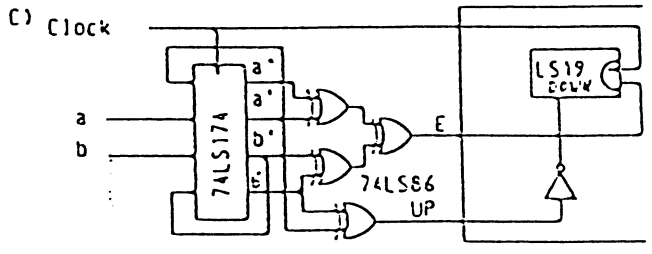


fig.11

This is the i/f method we use.

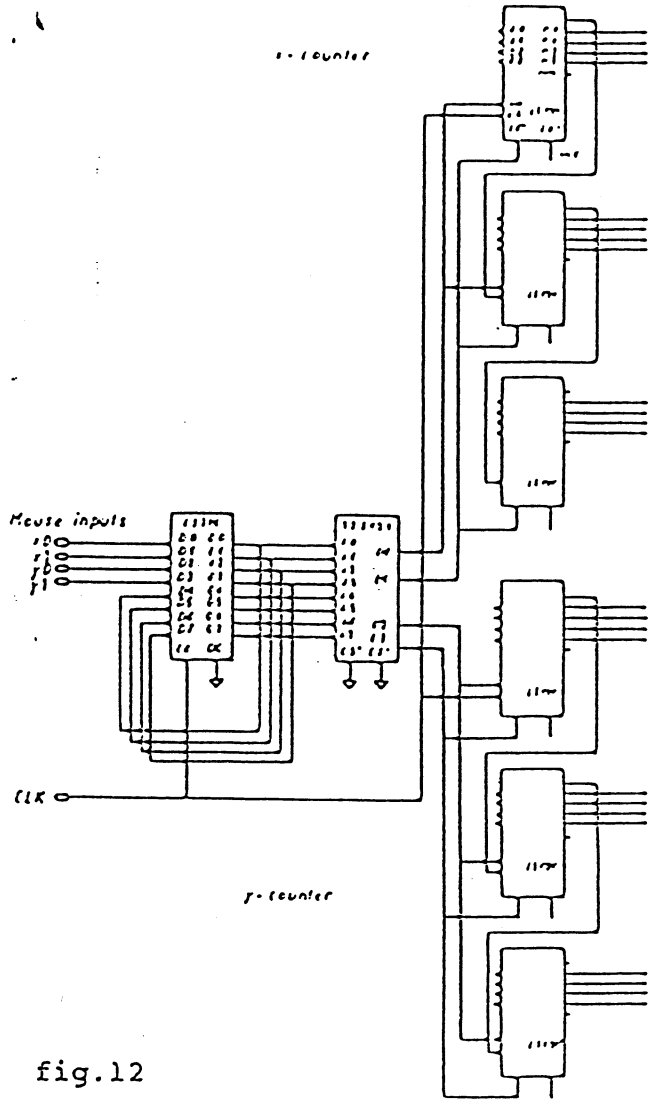
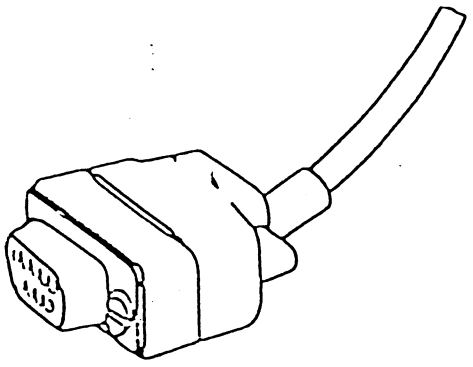


fig.12

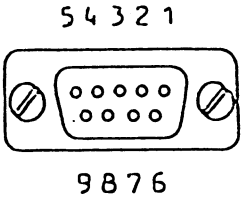
MOUSE D 83/H

Mouse D 83/H has the same mechanical features as the Mouse D 83/P The difference is that the 7 information bits are stored in a simple shift register and shifted out serially.Two timing signals (CP for clock pulse and LD for load pulse) define the shift frequency and the load of new information every 8 or 7 clock pulses.

The standard connector is a female 9 pins Cannon subminiature connector (fig.13).An 120 cm (4 feet) long, 5 wire cable is provided.



Cannon 2 DE 9P connector
Symbol on schematic



female plug
front view

Pin 1 + 5V	6 GND
2 y2	7 $\overline{M}$
3 y1	8 $\overline{D}$
4 x2	9 $\overline{G}$
5 x1	

fig.13

The full schematic es given in figure 14. It should be noticed that switches are not debounced. If a shift frequency greater than 10 kHz is used, there is some risk of transfer bounces. A lower frequency should not be used if very fast repositioning is expected.

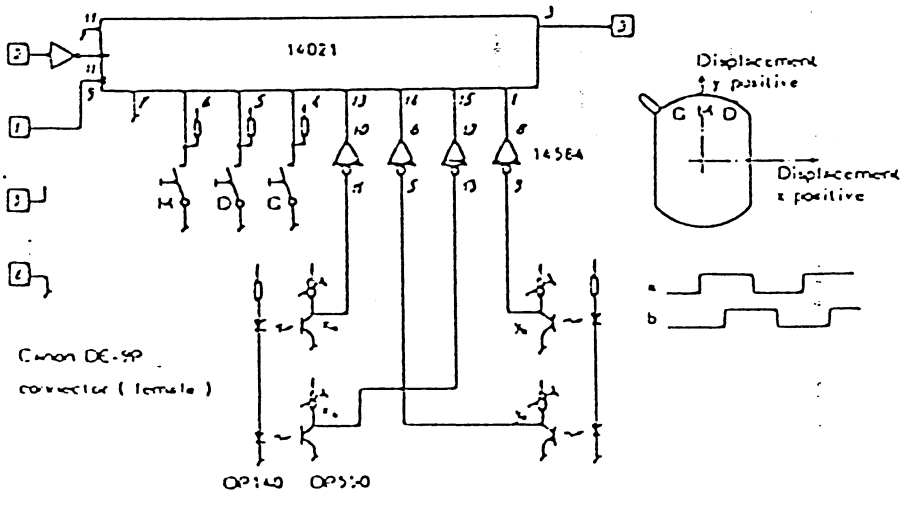
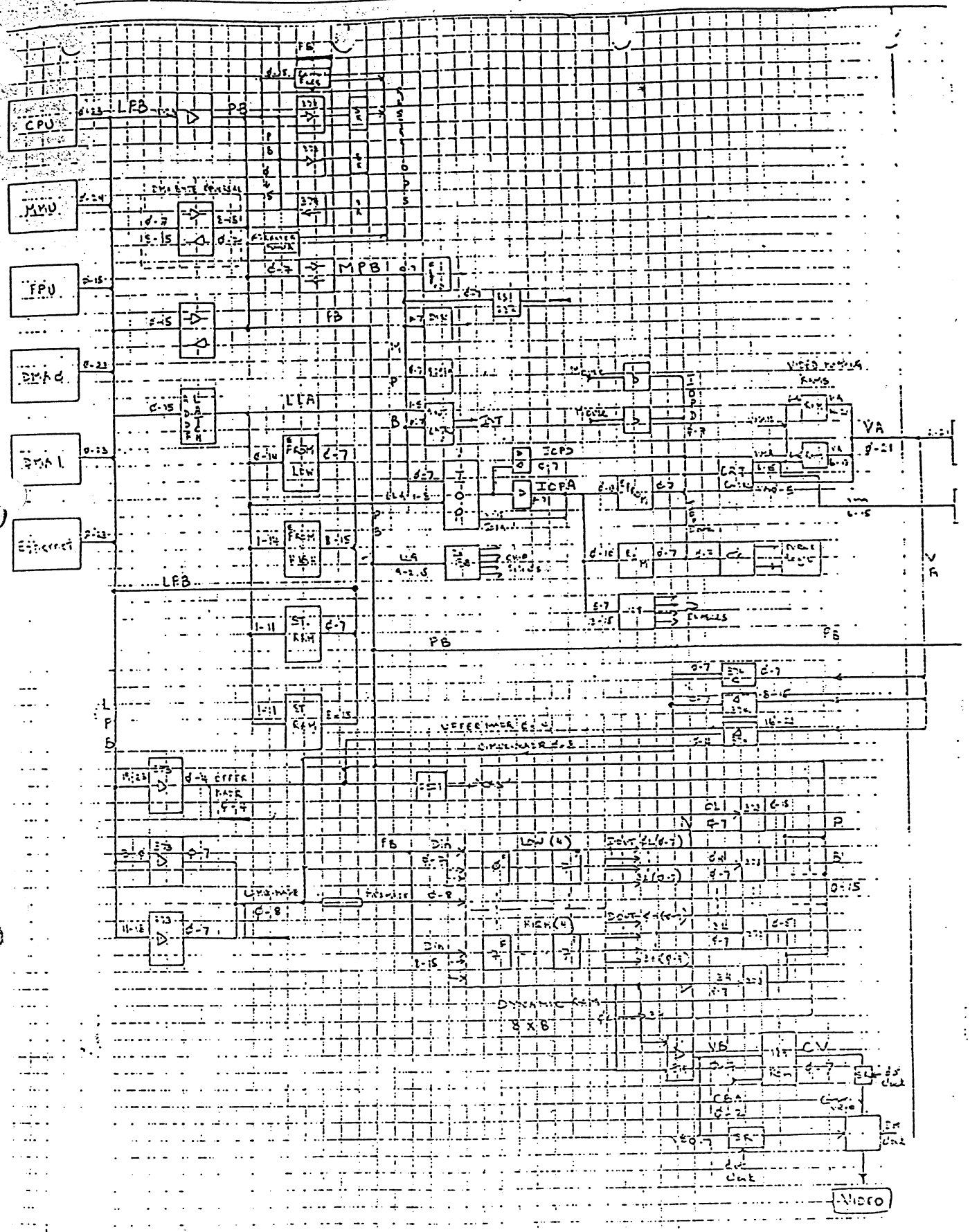


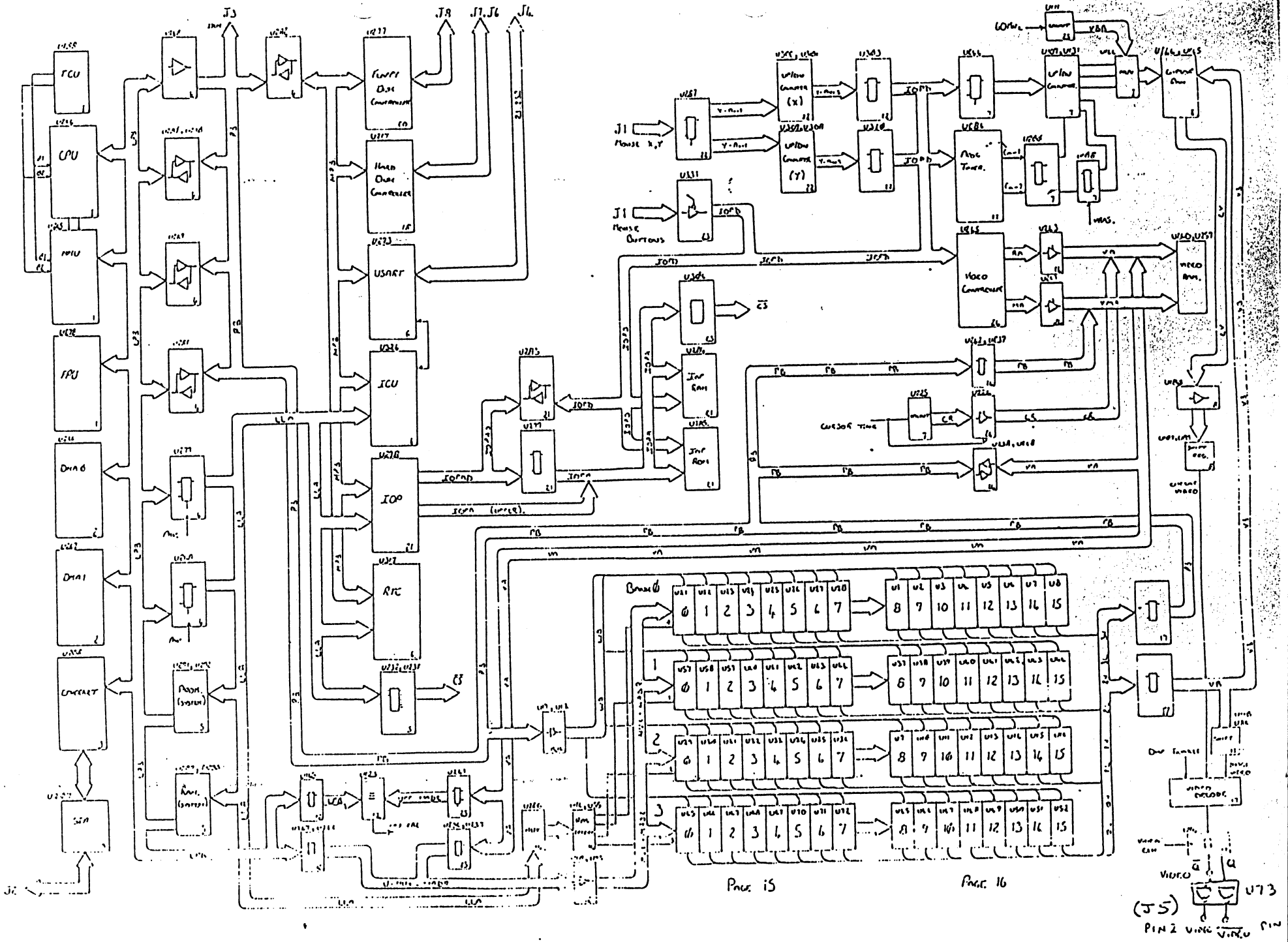
fig.14

SUPPORT NOTES NO. 26

Bus Structure of the MG-1

LH7ADJ


CPU
MMU
FPU
DMA
DMA
Ethernet
LPB
PB
MPB
FB
LCA
ICPA
ICPB
VA
VB
CV
CBA
Video
DYNAMIC RAM
8 X 8


FCU
CPU
MMU
FPU
DMA0
DMA1
CONCERT
SCA
Floppy Disk Controller
Hard Disk Controller
USART
ICU
IOP
RTC
Mouse (system)
Kbd. (system)
J3
J8
J7, J6
J4
J1
Mouse X,Y
J1
Mouse Buttons
Window Controller (X)
Window Controller (Y)
Video Timer
Video Controller
Video Ram
Video Decoder
Cursor Time
Inp Ram
Inp Ram
Page 15
Page 16
Video
(J5)
U73
Pin 2 using U1/U2 pin

SUPPORT NOTES NO. 15

Memory Addressing on the MG-1

CAUTION - This document must be read fully before commencing addressing adjustments.

The WCW MG-1 can be configured to accomodate various types of memory components (either 64K Dram's or 256K Dram's) located in the three types of boards and to construct the MG-1's.

Main Baord	0.5mb (64 K) memory
0.5mb expansion memory	0.5mb (64 K) memory
2mb expansion memory	2.0mb (256K) memory

The limitations, currently, on the use of these components is as follows:-

A) GENIX and FOS only recognise a maximum of 4mbytes.

B) A maximum of 4 expansion memory boards can be used.

However, additional information is included in this support note on layer memory array for future use.

The 0.5mb expansion memory board is currently capable of being addressed from 0mb to 4.0mb, also the 2.0mb expansion memory board from 0mb to 8mb.

Expansion memory board part numbers.

0.5mb board WCW part number W013 006 000
2.0mb Board WCW part number CA10030-2/256FU

1. Main board Links

This is carried out by adding or removing links (WCW part number W006 051 000) to the pins of patch connector P4, located between IC's U147 and U148 on the main board (Issue B)

The P4 patch connection pins are designated as follows when viewed from the front of the system.

2	4	6	8	10	12	14	16
1	3	5	7	9	11	13	15

Specified off and even numbers are connected together main board memory address's are from 0 to 7FFFF .

A) main board use inconjunction with 0.5mb expansion memory boards.

1 - 2	Linked
3 - 4	Linked
5 - 6	Linked
7 - 8	Linked
9 -10	Not linked

11- 12	Linked
13- 14	Linked
15- 16	Linked

B) Main board used inconjunction with 2.0mb expansion memory boards only.

1 - 2	Linked
3 - 4	Linked
5 - 6	Linked
7 - 8	Linked
9 - 10	Linked
11 - 12	Linked
13 - 14	Linked
15 - 16	Linked

This method disables the 0.5mb of memory as the main board so allowing a maximum of 4mbytes of memory to be installed by the use of two 2.0 mb expansion memory boards which are individually addressed.

C) Main board used inconjunction with a mixed population of 0.5mb and 2.0mb expansion memory board (To a maximum of 4 expansion memory board

1 - 2	Linked
3 - 4	Linked
5 - 6	Linked
9 - 10	Not linked
11 - 12	Linked
13 - 14	Not linked
15 - 16	Linked

This method enables the o.5mb of memory on the main board so allowing a maximum of 4mbytes of memory to be installed by the use of one expanson memory board and up to three 0.5mb expansion memory boards.

2) 0.5mbyte expansion memory links

Addressing of the 0.5mb expansion memory boards is arrived at by adding or removing links to the pins of the patch connection P1 of the expansion memory board. When the expansion memory board is installed in the main board and the links are viewed from the front of the system the links are designated as follows:

13	11	9	7	5	3	1
14	12	10	8	6	4	2

Maximum memory capacity	Memory address	Item
0.5mb	0 to 7FFFF	Main Board
1.0mb	80000 to FFFFF	1st 0.5mb Expansion memory board
1.5mb	100000 to 17FFF	2nd " " "
2.0mb	180000 to 1FFFFF	3rd " " "
2.5mb	200000 to 27FFFF	4th " " "
3.0mb	280000 to 2FFFFF	5th " " "
3.5mb	300000 to 37FFFF	6th " " "
4.0mb	380000 to 3FFFFF	7th " " "

NOTE : Only a maximum of 4 expansion memory boards can be inserted in a M-1.

The 0.5mb expansion memory patch connector P1 has all its links linked, except for the following list of connections which are not linked, so giving the 0.5mb expansion memory its correct addressing. (The table below gives the start and end address's for the expansion memory with the numbers of the links that are not linked for that address)

0.5 to 1mb	5 - 6
1.0 to 1.5mb	9 - 10
1.5 to 2.0mb	5 - 6,9 - 10
2.0 to 2.5mb	13 - 14
2.5 to 3.0mb	5 - 6,13 - 14
3.0 to 3.5mb	9 - 10,13 - 14
3.5 to 4.0mb	5 - 6, 9 - 10, 13 - 14

3) 2.0mb expansion memory board links

Addressing of the 2.0mb expansion memory boards is carried out by adding or removing links to the pins of the patch connection P1 of the expansion memory board.

(Reference should as so be made to the links of P4 on the main board details of which are given earlier in this support note)

a) 2.0mb expansion memory boards ONLY.

Maximum memory Capacity	Memory Adress	Items
2.0mb	0 to 1FFFFF	1st 2.0mb expansion board
4.0mb	2000000 to 3FFFFF	2nd 2.0mb expansion board
6.0mb	4000000 to 5FFFFF	3rd 2.0mb expansion board
8.0mb	6000000 to 7FFFFF	4th 2.0mb expansion board

NOTE : memory capacities above 4mb are currently not available, and the addressing of memory arrays are shown only for future feference.

The 2.0mb expansion memory patch connector P1 has all its links, except for the following list of connections which are not linked, so giving the 2.0mb. expansion memory its correct addressing (the table below gives the start and end address for the expansion memory with the number of the links that are not linked for the address)

0 to 2.0mb	3 - 4, 5 - 6, 7 - 8, 9 - 10
2.0 to 4.0mb	3 - 4, 5 - 6, 7 - 8, 9 - 10, 13 - 14
4.0 to 6.0mb	1 - 2, 3 - 4, 5 - 6, 7 - 8, 9 - 10
6.0 to 8.0mb	1 - 2, 3 - 4, 5 - 6, 7 - 8, 9 - 10, 13 - 14

4) Mixed configuration of memory boards

Example

4 Mbytes with the use of main board, one 2.0mb and three 0.5mb expansion memory boards.

Memory Adress	Memory Physical location	Support note paragraph
0 to 7FFFF	0.5mb main board	See 1c
80000 to 27FFFF	2.0mb Expansion memory board	See 3
280000 to 2FFFFFF	0.5mb " " "	See 2
300000 to 37FFFF	0.5mb " " "	See 2
380000 to 3FFFFF	0.5mb " " "	

Total memory = 4Mbytes

MEMORY EXPANSION CARDS ADDRESS PATCHING. (P1).

½ Mb EXPANSION.	ADDRESS	LINKS P1 *						
	Mb.	1-2	3-4	5-6	7-8	9-10	11-12	13-14
	½ - 1	IN	IN	OUT	IN	IN	IN	IN
	1 - 1½	IN	IN	IN	IN	OUT	IN	IN
	1½ - 2	IN	IN	OUT	IN	OUT	IN	IN
	2 - 2½	IN	IN	IN	IN	IN	IN	OUT
	2½ - 3	IN	IN	OUT	IN	IN	IN	OUT
	3 - 3½	IN	IN	IN	IN	OUT	IN	OUT
	3½ - 4	IN	IN	OUT	IN	OUT	IN	OUT
	4 - 4½	OUT	IN	IN	IN	IN	IN	IN
	4½ - 5	OUT	IN	OUT	IN	IN	IN	IN
	5 - 5½	OUT	IN	IN	IN	OUT	IN	IN
	5½ - 6	OUT	IN	OUT	IN	OUT	IN	IN
	6 - 6½	OUT	IN	IN	IN	IN	IN	OUT
	6½ - 7	OUT	IN	OUT	IN	IN	IN	OUT
	7 - 7½	OUT	IN	IN	IN	OUT	IN	OUT
	7½ - 8	OUT	IN	OUT	IN	OUT	IN	OUT
2 Mb EXPANSION	Mb							
	0 - 2	IN	OUT	OUT	OUT	OUT	IN	IN
	2 - 4	IN	OUT	OUT	OUT	OUT	IN	OUT
	4 - 6	OUT	OUT	OUT	OUT	OUT	IN	IN
	6 - 8	OUT	OUT	OUT	OUT	OUT	IN	OUT

* ON ISSUE 'C' MEMORY EXPANSION CARDS P1 IS INSERTED IN THE OPPOSITE DIRECTION TO THE EARLIER EXPANSION CARDS.

MAIN BOARD P4

	ADDRESS/Mb	LINK P4							
½ Mb ON BOARD MEMORY ISSUE B.	Mb	1-2	3-4	5-6	7-8	9-10	11-12	13-14	15-16
ENABLED.	0 - ½.	IN	IN	IN	IN	OUT	IN	IN	IN
"	2 - 2½	IN	IN	IN	IN	OUT	IN	OUT	IN
"	4 - 4½	IN	IN	IN	IN	OUT	OUT	IN	IN
"	6 - 6½	IN	IN	IN	IN	OUT	OUT	OUT	IN
DISABLED	—	IN	IN	IN	IN	IN	IN	IN	IN
½ Mb ON BOARD MEMORY ISSUE C.									
ENABLED	0 - ½	IN	IN	IN	IN	IN	IN	IN	OUT
"	2 - 2½	IN	IN	IN	IN	OUT	IN	IN	OUT
"	4 - 4½	IN	IN	IN	IN	IN	OUT	IN	OUT
"	6 - 6½	IN	IN	IN	IN	OUT	OUT	IN	OUT
DISABLED	—	IN	IN	IN	IN	IN	IN	IN	IN
2Mb ON BOARD MEMORY. ISSUE C									
	0 - 2	OUT	OUT	OUT	OUT	IN	IN	IN	OUT

SUPPORT NOTES NO.23

Keyboard on the MG-1

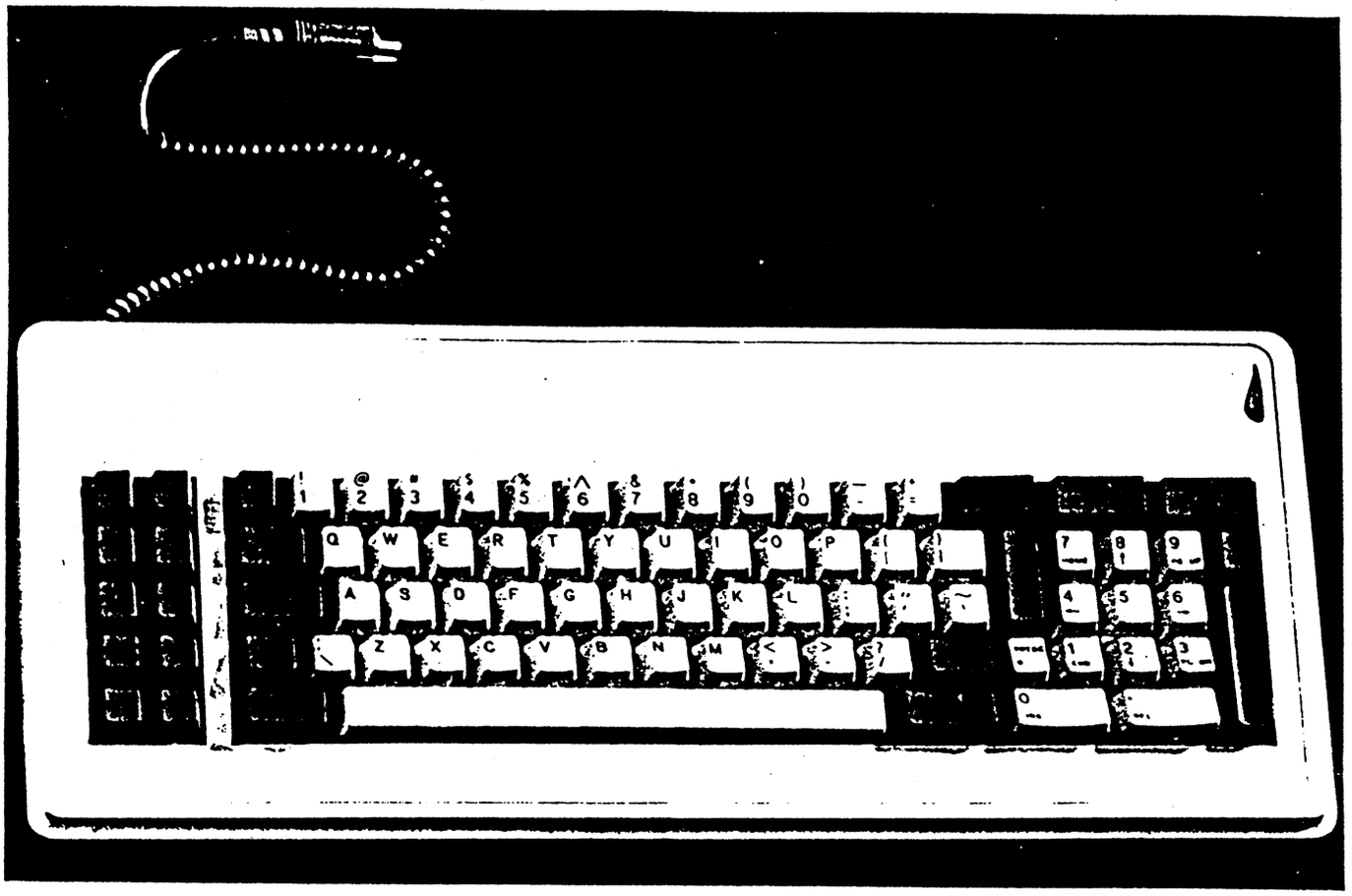
JF3AAK

GENERAL INSTRUMENT

Computer Products Division
C.P. Clare International N.V.

Data sheet E501-1083

PERSONAL COMPUTER KEYBOARD



STANDARD FEATURES

- 83 station full travel keyboard
- Ergonomic capacitive switch technology to meet the 30 mm requirement
- Linear feel
- Microprocessor intelligence
- 4 mode full ASCII character set
- Capslock, numlock, alt key
- N-key rollover
- Sculptured keytops
- Auto repeat

OPTIONAL FEATURES

- Baud rate selection
- RS422 output
- IBM interface
- + 12 V power input
- Telephone header
- Full keycode reassignment
- National versions

MECHANICAL DATA

• Key total travel	3,5 mm
• Key operating travel	1,77 mm
• Key actuating force	70 gr
• Keytop colour	Beige shell, black legends Light brown shell, black legends
• Frame	C.R.S. - 1,5 mm Anti-corrosive treatment
• PCB	FR4 quality grade Double side PCB, Plating through holes
• Swith operating life	100.10^6 cycles

ELECTRICAL DATA

• Serial output data	1 start bit 8 data bits Odd parity bit • 2 stop bits 300 baud transmission rate

OPTIONS

1. Transmission rate :
   300 baud: standard
   1200 baud: cut jumper NW
   2400 baud: cut jumper SW
   9600 baud: cut jumper NW and SW

2. Full keycode reassignment provided through eprom exchange. Keycodes reside in pages, one page per keyboard mode. Absolute keycode addresses are obtained by adding the page offset value to the basic switch address (ref. code table).

   Page offset:
   - Unshift mode: 300 H
   - Shift mode: 380 H
   - Control mode: 200 H
   - Shift/control mode: 280 H

3. RS 422:
   Install Z5 (DS3692), remove Z6 (74LS125)

4. Power input = + 12 V DC:
   Cut jumper XY
   Install VR1 (7805)

5. IBM interface:
   Z4 = 106642-00 (= ordering ref.)

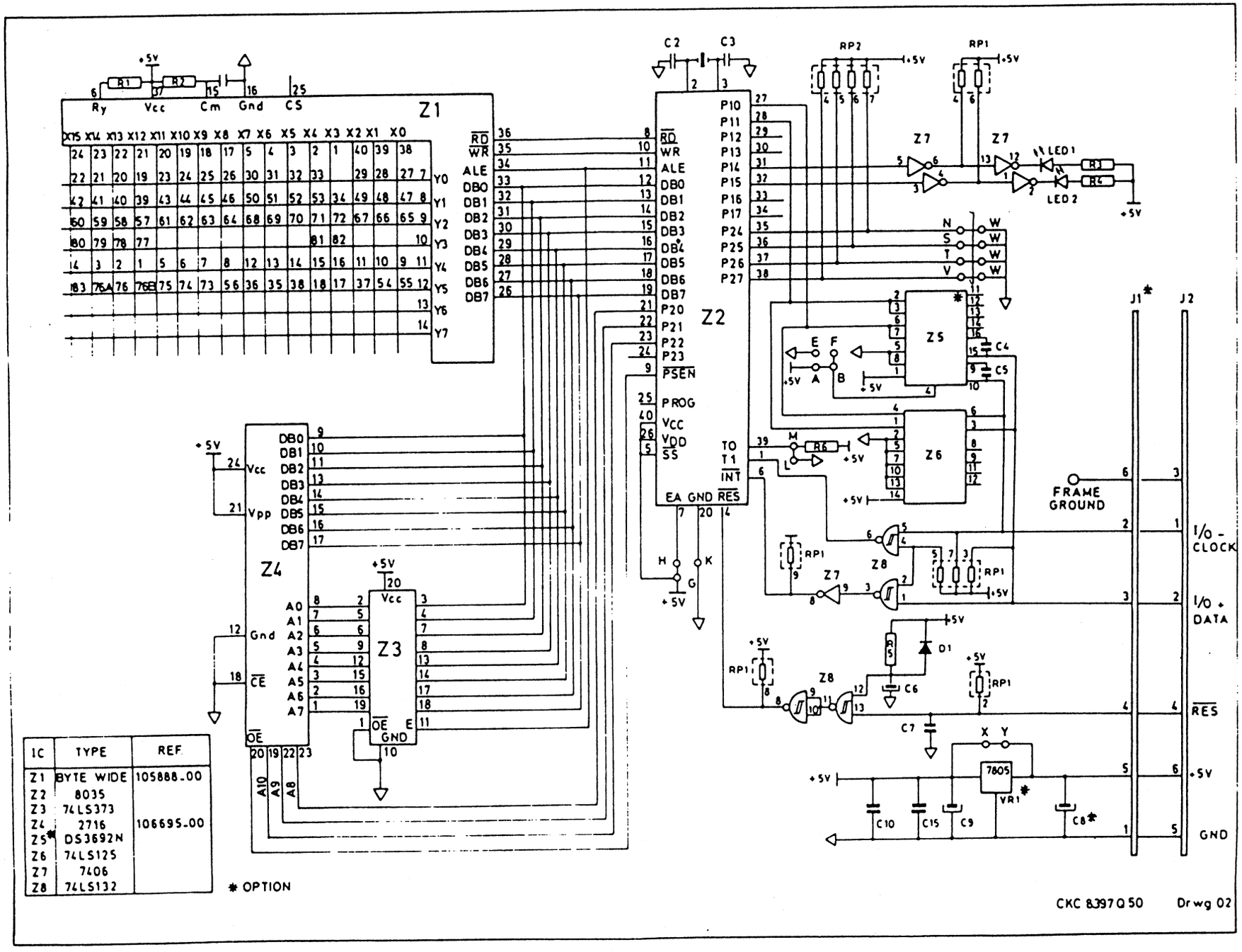
make/Break codes

CONNECTOR DETAIL

J1	J2	FUNCTION TTL	FUNCTION RS 422	FUNCTION IBM
1	5	GROUND	GROUND	GROUND
2	1	OUTPUT	OUT —	I/O —
3	2	—	OUT +	I/O +
4	4	RESET	RESET	RESET
5	6	+ 5 V DC	+ 5 V DC	+ 5 V DC
6	—	FRAME GND	FRAME GND	FRAME GND

J1 = Telephone header (option)
J2 = 6 pin strip, 2,54 mm spacing (STD)

DIAGRAM



IC	TYPE	REF.
Z1	BYTE WIDE	105888-00
Z2	8035	
Z3	74LS373	
Z4	2716	106695-00
Z5*	DS3692N	
Z6	74LS125	
Z7	7406	
Z8	74LS132	

* OPTION

FPB

1

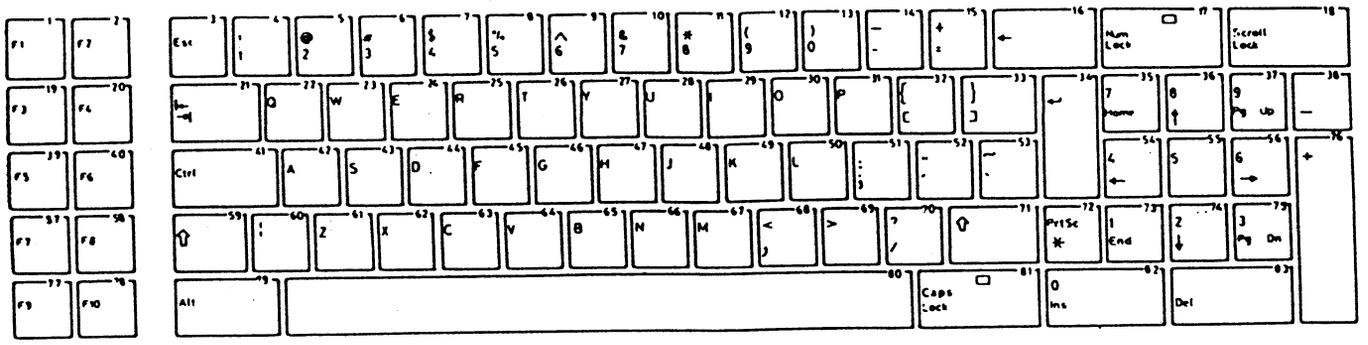
2

3

5

4

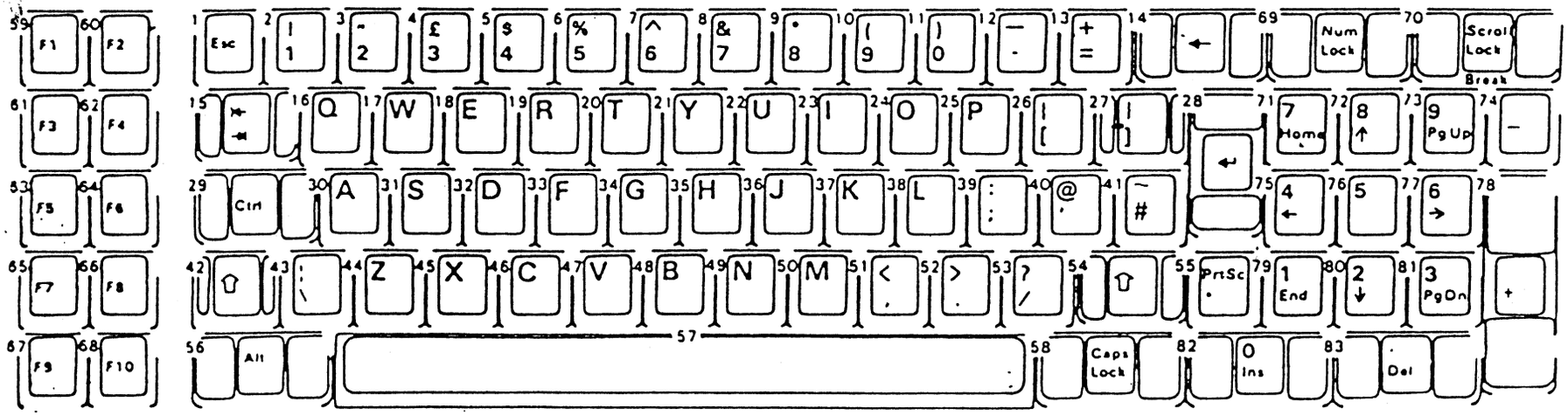
KEYTOP LAYOUT



ASCII CODE TABLE

KEY	SWITCH ADDRESS (HEX)	UNSHIFT	SHIFT	CONTROL	CONTROL AND SHIFT
1	4C	80	80	80	80
2	4D	81	81	81	81
3	4E	1B	1B	1B	1B
4	4F	31	21	31	21
5	4B	32	40	32	00
6	4A	33	23	33	23
7	49	34	24	34	24
8	48	35	25	35	25
9	40	36	5E	36	1E
10	41	37	26	37	26
11	42	38	2A	38	2A
12	47	39	28	39	28
13	46	30	29	30	29
14	45	2D	5F	1F	1F
15	44	3D	2B	3D	2B
16	43	08	08	08	08
17	53		NUM LOCK		
18	54	8B	8B	8B	8B
19	0C	82	82	82	82
20	0D	83	83	83	83
21	0E	09	89	09	89
22	0F	71	51	11	11
23	0B	77	57	17	17
24	0A	65	45	05	05
25	09	72	52	12	12
26	08	74	54	14	14
27	00	79	59	19	19
28	01	75	55	15	15
29	02	69	49	09	09
30	07	6F	4F	0F	0F
31	06	70	50	10	10
32	05	5B	7B	1B	1B
33	04	5D	7D	1D	1D
34	13	0D	0D	0D	0D
35	56	B7	37	B7	37
36	57	11	38	11	38
37	52	B9	39	B9	39
38	55	2D	2D	2D	2D
39	1C	84	84	84	84
40	1D	85	85	85	85
41	1E		CTRL		
42	1F	61	41	01	01

KEY	SWITCH ADDRESS (HEX)	UNSHIFT	SHIFT	CONTROL	CONTROL AND SHIFT
43	1B	73	53	13	13
44	1A	64	44	04	04
45	19	66	46	06	06
46	18	67	47	07	07
47	10	68	48	08	08
48	11	6A	4A	0A	0A
49	12	6B	4B	0B	0B
50	17	6C	4C	0C	0C
51	16	3B	3A	3B	3A
52	15	27	22	27	22
53	14	60	7E	60	7E
54	51	12	34	12	34
55	50	35	35	35	35
56	58	13	36	13	36
57	2C	86	86	86	86
58	2D	87	87	87	87
59	2E		SHIFT		
60	2F	5C	7C	1C	1C
61	2B	7A	5A	1A	1A
62	2A	78	58	18	18
63	29	63	43	03	03
64	28	76	56	16	16
65	20	62	42	02	02
66	21	6E	4E	0E	0E
67	22	6D	4D	0D	0D
68	27	2C	3C	2C	3C
69	26	2E	3E	2E	3E
70	25	2F	3F	2F	3F
71	24		SHIFT		
72	23	2A	AA	2A	AA
73	59	B1	31	B1	31
74	5A	14	32	14	32
75	5B	B3	33	B3	33
76	5D	2B	2B	2B	2B
77	3C	88	88	88	88
78	3D	8A	8A	8A	8A
79	3E		ALT		
80	3F	20	20	20	20
81	34		CAPS LOCK		
82	33	B0	30	B0	30
83	5F	7F	2E	7F	2E



NOTE

1 NOMENCLATURE IS ON BOTH TOP AND FRONT FACE OF KEYBUTTON AS SHOWN.
THE NUMBER TO THE UPPER LEFT DESIGNATES THE BUTTON POSITION.