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Changing M32632 to "NS32016"

You should start with an FPGA which is large enough to hold the module "example" which you found in example.v . Then you see how large it is and how far you are away from your target FPGA. It may be good to have the architecture_v10.pdf documentation near you. (Note: "..." is always a module name.)

1. Delete the FPU

a) Take out the instance "SP_FPU" in the module "DATENPFAD" (source file DATENPFAD.v) . The outputs of "SP_FPU" must be set to a defined value. For example the output FP_OUT : **assign FP_OUT = 32'd0;** . It is also possible to set them to zero where they are used but this may be more time consuming to change. To find the outputs of "SP_FPU" look in the source code file SP_FPU.v .

b) Take out the instance "DFPU_ADDSUB" in the module "DP_LOGIK" . The source code of both modules is located in the file DP_FPU.v . Again set the outputs to 0.

c) Do the same like in b) with the instances "DFPU_MISC" and "DFPU_MUL" .

d) Use **assign fpout = 70'd0;** instead of **casex** statement in "DP_LOGIK" .

e) Use **assign MRESULT = {21'd0,MDA[31:0]} * {21'd0,MDB[31:0]};** in "DP_FPU" instead of **assign MRESULT = MDA * MDB; .** The module is located in the file DP_FPU.v .

2. Delete the Coprocessor Interface

In the module "example" the inputs of the Coprocessor interface at M32632 should be set to 0. Take out the coprocessor of the example.

3. Delete the Caches and the MMU

Here a different strategy shall be used. It is very complicated to take the logic out. Instead we hope that the FPGA vendor tools do the job for us. Let's start with the most important input pin of M32632: the "ENable DRAM" input (ENDRAM) . This input pin will allow DRAM access if set high. An active DRAM interface enables the caches and the MMU although software must finally switch them on. If ENDRAM is fixed low all accesses are directed to the IO interface. Therefore we set the ENDRAM input at the "M32632" in "example" to 1'b0 . Next we delete everything that is connected to the DRAM pins of "M32632". In "example" it is the module "ex_dram_emul" . The DRAM inputs of "M32632" are as usual set to 0.

In case that this action will not help much we can set other pins as well. Set the inputs CFG (2 bits wide) and MCR_FLAGS (4 bits wide) of the modules "DCACHE" and "ICACHE" to 0 in the module "M32632".

If you still find the memory blocks of the caches in the ressource list you should take them out manually in the files DCACHE.v and ICACHE.v . If the caches and the MMU are not used there is no need for any memory block. Set their outputs to 0.

4. Miscellaneous

Limit the use of the external IO_A bus to [23:0] instead of [31:0] .